Steady State Load Models for Power System Analysis

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Abstract

The last full review of load models used for power system studies occurred in the 1980s. Since then, new types of loads have been introduced and system load mix has changed considerably. The examples of newly introduced loads include drive-controlled motors, low energy consumption light sources and other modern power electronic loads. Their numbers have been steadily increasing in recent years, a trend which is expected to escalate. Accordingly, the majority of load models used in traditional power system studies are becoming outdated, as they are unable to accurately represent power demand characteristics of existing and future loads. Therefore, in order to accurately predict both active and non-active power demand characteristics of aggregated modern power system loads in different load sectors (e.g. residential, commercial or industrial), existing load models should be updated and new models developed.

This thesis aims to fill this gap by developing individual, generic and aggregated steady state models of the most common loads in use today, as well as of those expected to show significant growth in the future. The component-based approach is adopted for load modelling, where individual load models are obtained in detailed simulations of physical devices. Whenever possible, the developed individual load models are validated by measurements. These detailed individual load models are then simplified and expressed as equivalent circuit and analytical models, which allowed the establishment of generic load models that can be easily aggregated. It should be noted that since all non-active power characteristics are correctly represented, the developed aggregated load models allow for a full harmonic analysis, which is not the case with the standard steady state load models. Therefore, the proposed load models form an extensive library of comprehensive load models that are suitable for use in multiple areas of power system research.

Based on the results of research related to typical domestic/residential sector load mix, the newly developed load models are aggregated and then applied to a typical UK/Scotland distribution network. Considerable differences are seen between network characteristics of newly proposed and previously developed models. The voltage distortion of a typical distribution system bus is investigated, and it is shown that distortion of the system voltage is likely to increase significantly in the future. The results of the presented research also suggest that neglecting the harmonic characteristics from the set of general load attributes may introduce errors in standard load flow studies.

Declaration of originality

I hereby declare that the research recorded in this thesis and the thesis itself was composed and originated entirely by myself in the Department of Electrical Engineering at The University of Edinburgh.

Charles Cresswell

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Acronyms and abbreviations

ac	alternating current
ASD	adjustable speed drive (three-phase)
BERR	Department for Business, Enterprise and Regulatory Reform
CF	crest factor
CFL	compact fluorescent lamp
CFT	compact fluorescent tube
CSR	capacitive start and run
CSIR	capacitive start - inductive run
dc	direct current
DEFRA	Department for Environment, Food and Rural Affairs
DF	diversity factor
DIAC	diode for alternating current
DSM	demand side management
DTC	direct torque control
DTI	Department of Trade and Industry (now BERR)
EMI	electromagnetic interferance
EPRI	Electric power research institute
EU	European union
FOC	field orientated control
GIL	general incandescent lamp
ICT	Information and communication technology
LED	light emitting diode
LFL	linear fluorescent lamp
LFT	linear fluorescent tube
LMC	load meeting capacity
MMF	magnetomotive force
NTC	negative temperature coefficient
PC	personal computer
PFC	power factor correction
PSS/E	power system simulator for engineering
pu	per unit
PWM	pulse width modulated
RMS	root mean square
RSIR	resistive start-inductive run

SASD	single-phase adjustable speed drive
SMPS	switch mode power supply
SPIM	single-phase induction motor
SVC	space vector control
THD	total harmonic distortion
UKGDS	United Kingdom Generic Distribution Systems
V/Hz	volt-hertz control
VSI	voltage source inverter

Nomenclature

A_p	aggregate load active power coefficient (polynomial model)
A_q	aggregate load reactive power coefficient (polynomial model)
a_f	frequency sensitivity parameter
a_n	load type coefficient
a_{1-4}, b_{1-4}	tube model coefficients
C_{dc}	dc link capacitor
C_{emi}	emi filter capacitance
C_{mag}	capacitance in magnetic ballast
c_n	percentage contribution of load type
f	system frequency at considered bus
f_o	nominal system frequency at considered bus
h	harmonic order
I	rms current
$I_{dc,hf}$	cycle-by-cycle rms voltage
I_p	active power coefficient of current in polynomial model
I_q	reactive power coefficient of current in polynomial model
I_t	rms tube current
i	instantaneous current
i_{dc}	instantaneous dc link current
$i_{dr}^{'}$	referred d-axis rotor current (dq mod. of 3-phase ind. motor)
i_{ds}	d-axis stator current (dq mod. of 3-phase ind. motor)
$i_{qr}^{'}$	referred q-axis rotor current (dq mod. of 3-phase ind. motor)
i_{qs}	q-axis stator current (dq mod. of 3-phase ind. motor)
L_{dc}	dc link inductor
L_{emi}	inductance of emi filter
$L_{lR}^{'}$	auxiliary rotor winding referred leakage inductance (dq mod. of 1-phase ind. motor)
$L_{lr}^{'}$	main rotor winding referred leakage inductance (dq mod. of 1-phase ind. motor)
L_{lS}	auxiliary stator winding leakage inductance (dq mod. of 1-phase ind. motor)
L_{ls}	main stator winding leakage inductance (dq mod. of 1-phase ind. motor)
L_m	magnetising inductance (dq mod. of 3-phase ind. motor)
L_{mag}	inductance in magnetic ballast
L_p	primary leakage inductance
$L_r^{'}$	referred rotor leakage inductance (dq mod. of 3-phase ind. motor)
L_s	stator leakage inductance (dq mod. of 3-phase ind. motor)

L_{sys}	System inductance
N	non-active power
np	coefficient of active power in exponential load model
nq	coefficient of reactive power in exponential load model
P	active power demand
P_1	fundamental active power
PF	true power factor
PF_1	displacement power factor
PF_d	distortion power factor
P_H	harmonic active power
P_o	nominal active power demand
P_p	active power coefficient of power in polynomial model
P_q	reactive power coefficient of power in polynomial model
P_t	tube power
Q	reactive power demand (sinusoidal conditions)
Q_1	fundamental reactive power
Q_o	nominal reactive power demand (sinusoidal conditions)
$R_{b,CFL}$	base resistance for CFL equivalent resistance model
R_{eq1}	equivalent resistance during discharge period (CFL)
R_{eq1}	equivalent resistance during charge period (CFL)
R_{dc}	equivalent resistance at rectifier dc link
R_{diode}	diode resistance
R_{sys}	system resistance
R_t	tube resistance
$r_R^{'}$	auxiliary rotor winding referred resistance ((dq mod. of 1-phase ind. motor)
r_r^1	referred rotor winding resistance (dq mod. of 3-phase/1-phase ind. motor)
r_S	auxiliary stator winding resistance (dq mod. of 1-phase ind. motor)
r_s	stator winding resistance (dq mod. of 3-phase/1-phase ind. motor)
S	apparent power
S_1	fundamental apparent power
S_H	harmonic apparent power
S_N	non-fundamental apparent power
t	time
t_{hu}	specified SMPS hold-up time
V	rms voltage
V_{diode}	diode forward voltage drop
V_{line}	rms line voltage
V_{phase}	rms phase voltage
V_t	rms tube voltage

v	instantaneous voltage
v_{dc}	instantaneous dc link voltage
$v_{dc,nom}$	nominal dc link voltage
$v_{dc,min}$	minimum operating voltage of SMPS
v_{ds}	d axis stators voltage (dq mod. of 3-phase ind. motor)
v_{qs}	q axis stators voltage (dq mod. of 3-phase ind. motor)
v_{rect}	instantaneous rectified system voltage
$v_{rip,max}$	maximum value of dc link ripple voltage
$v_{rip,min}$	minimum value of dc link ripple voltage
v_{start}	dc link voltage at start of discharge period
X	reactance
Z	system impedance
Z_p	active power coefficient of impedance in polynomial model
Z_q	reactive power coefficient of impedance in polynomial model
ω	rotational speed (radians)
ω_r	motor rotational speed
θ	phase angle
τ	mechanical torque
η	effeciency

Chapter 1
Introduction

For a long time, it has been recognised that the operation and performance of electricity supply systems are strongly influenced by the characteristics of the supplied load, [1]. Accordingly, the selection of the load model in a particular power system study will have a significant effect on the results of the study and, therefore, corresponding design decisions. Too optimistic load models can lead to inadequate system design or reinforcement, and may result in either costly upgrades or insecure systems, more vulnerable to various types of disturbances and collapse. Too pessimistic load models can, on the other hand, lead to unnecessary capital expenditure and uneconomical operation of the supply system. In the past, more pessimistic load models have often been favoured, in order to accommodate conservative safety and design margins. However, the most pessimistic load representation is sometimes hard to determine. Supply systems are increasingly being operated near to their operational margins, due to growing demand, economic and environmental pressures to run these systems close to their maximum capacity. Representative and accurate load models are thus becoming increasingly important for correct assessment of network performance. In addition, accurate load models can facilitate better decision making in relation to financial investment.

Traditionally, load models have been developed for use in high and medium voltage studies, with low voltage distribution systems and associated loads represented as a combined single (i.e. aggregate) load model. Accordingly, these aggregate loads are relatively insensitive to variations in characteristics of individual loads. However, the move away from centralised to distributed generation of electricity requires distribution networks to be considered in more detail. This also means that distribution system load should be considered in greater detail. When representing these smaller aggregate distribution system loads, the characteristics of individual load components become more important, and should be given more attention than has been the case previously.

Load models will play an increasingly important role in system design and planning. A major reason for this is the anticipated higher penetration of distributed generation and subsequent need for more efficient management of distribution networks. For example, it has been shown in [2] that system load characteristics will strongly affect optimal location, size and financial feasibility of distributed generation. Furthermore, the types and numbers of loads commonly found in the distribution system have changed significantly in the last few decades, with most significant and most prominent increase of non-linear loads. This represents a major change in

load inventory, which should be taken into account when considering load models for use in studies of modern power supply systems.

Although the importance of accurate representation of system load is generally known, certain assumptions are often made about load models. This is due to the lack of, or uncertainty in, available load modelling data. Therefore, efforts in clarifying or presenting new load models are of general importance to all aspects of supply system design and operation.

1.1 Load modelling

In this thesis, the term "load" is defined as either a single device (or "load type") connected to the supply system, or an aggregation of load types connected to the supply system. A load model is mathematical or analytical representation of the changes in active and/or reactive power demand of a load, usually as a function of the changes in applied voltage and, in some cases, frequency. Load models can be generally defined as either static or dynamic. A static model is used to represent the active and reactive power demand of the load as a function of voltage and frequency at a particular instant in time. A dynamic load model represents active and reactive power demand as a function of voltage, frequency and time. Dynamic models are typically represented in the form of differential equations and used in voltage stability studies, studies of inter-area oscillations and long term stability studies. A commonly used dynamic load model is based on the equivalent circuit of an induction motor, [3]. This is because induction motor load represents a significant proportion of the total system load. According to [4], the lack of dynamic motor models in power system studies is often thought to be the main cause of differences in results between field-measurements and large-scale simulations. When static and dynamic models are used together, this is known as a composite dynamic load model, [5]. As the focus of this thesis is on static load models, dynamic models are not specifically considered in further text.

There are several commonly used static load models, [3]:

Constant impedance load model, for which active and reactive powers vary proportionally to the square of the voltage magnitude. This model is also sometimes called the "admittance model".

Constant current load model, for which active and reactive powers of the load vary in direct proportion (linearly) to the voltage magnitude.

Constant power load model, for which load will draw constant active and reactive power, irrespective of the changes in system voltage. This model is often referred to as "constant MVA model".

Exponential load model, which uses the exponents np and nq to define the relationship between active/reactive power demand and system voltage. When $np = nq = 2$, the load is a constant impedance load; when $np = nq = 1$ the load is a constant current load, and when $np = nq = 0$, the load is a constant power load. The exponents may also be set to any value, in order to represent the desired load characteristic:

$$P = P_o \left(\frac{V}{V_o} \right)^{np} \tag{1.1}$$

$$Q = Q_o \left(\frac{V}{V_o} \right)^{nq} \tag{1.2}$$

Polynomial load model, which represents the load as the sum of the constant impedance (Z), constant current (I) and constant power (P) load models, often referred to as the "ZIP model". As this model is of general quadratic form, it can provide better matching to non-linear load characteristics than the exponential load model.

$$P = P_o \left[Z_p \left(\frac{V}{V_o} \right)^2 + I_p \left(\frac{V}{V_o} \right) + P_p \right] \tag{1.3}$$

$$Q = Q_o \left[Z_q \left(\frac{V}{V_o} \right)^2 + I_q \left(\frac{V}{V_o} \right) + P_q \right] \tag{1.4}$$

Where: Z_p, I_p, P_p, Z_q, I_q, P_q are the polynomial model coefficients and for exponential and polynomial models, P and Q are the actual active and reactive power demands of the load, V is the actual voltage at the considered load bus, V_o is the nominal system voltage, P_o and Q_o are nominal values of active and reactive power of the load.

Frequency dependent load model, which can be used to add frequency dependency to either exponential or polynomial load models. This is achieved by multiplying the relevant exponential or polynomial load model with the frequency dependent term:

$$[1 + a_f (f - f_o)] \tag{1.5}$$

Where: f is the actual frequency at the considered bus, f_o is the nominal frequency and a_f is the frequency sensitivity parameter of the model.

1.1.1 Two general approaches to load modelling

Before the exponential or polynomial load models can be used in power system studies, the corresponding coefficients must be determined so that they represent the characteristics of the modelled load as accurately as possible. There are two commonly used approaches to obtain load models and values of the coefficients: 1) the measurement-based approach, and 2) the

component-based approach.

1.1.1.1 Measurement-based approach to load modelling

The measurement-based approach to load modelling is implemented by measuring the variation of active and reactive power with the changes in system voltage and frequency directly at the system bus/buses of interest. The corresponding changes in system bus voltage may either be the result of natural variations, or the result of intentional or unintentional disturbances. The measured data are then used to estimate the coefficients of the exponential or polynomial models. References [6], [7] and [8] give good examples of how this approach can be implemented. The advantage of this approach is that physical data from the actual system under study can be used. This should result in accurate load models. The main disadvantage of this approach is that significant financial investment is required to implement the measurements. The measurement must also be performed over a long period of time, so that seasonal and daily variations in load characteristics may be taken into account. Additionally, it is not always possible to determine how load will respond to major variation in the supply system. A further disadvantage is that the developed load models are likely to be valid only for the considered/measured bus or buses, where supplied loads are connected. Accordingly, these load models are relatively inflexible and cannot to be used to directly predict changes in load characteristics due, for example, to future changes in load inventory. However, the measurements based approach to load modelling is still one of the most accurate methods to model actual load characteristics.

1.1.1.2 Component-based approach to load modelling

The component-based approach to load modelling involves building the desired bus load model from the individual load models of devices connected to the system. This method was developed in research projects commissioned by Electric Power Research Institute (EPRI) from 1976 onwards, [9–12]. Figure 1.1 shows a diagrammatic representation of the component-based approach to load modelling. The component-based approach requires three sets of data, [13]:

1. Load sector mix - This gives the percentage contributions of each load sector to total load bus power.
2. Load mix - This gives the percentage contributions of each load type to the particular load sector.
3. Load characteristics - This gives the characteristics of the individual load type and, where relevant, sub-type, i.e. individual load models.

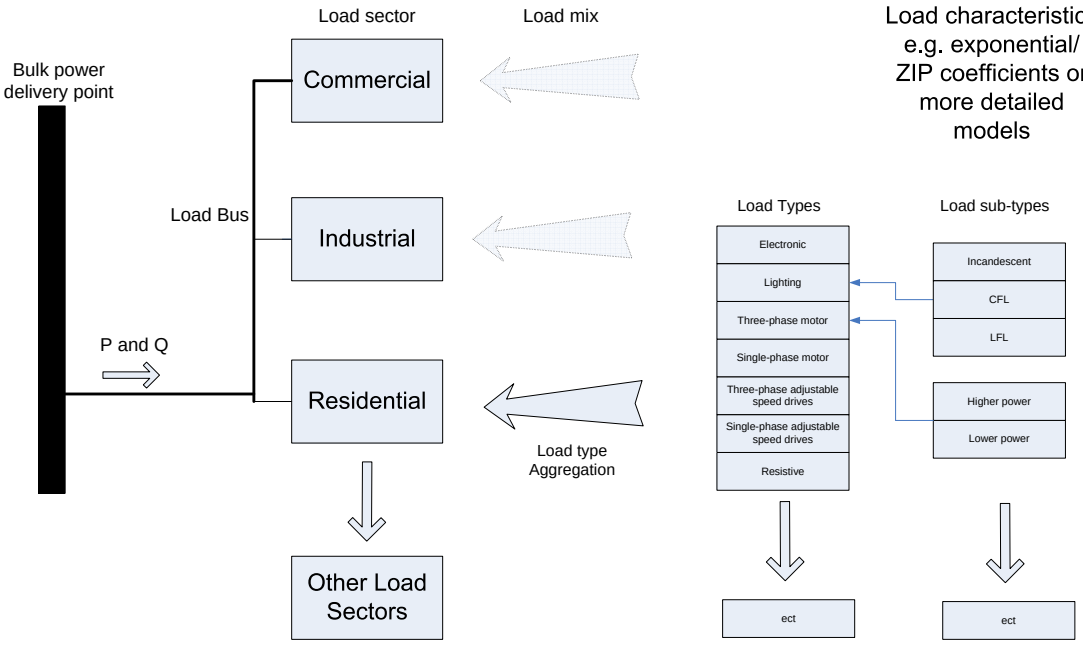


Figure 1.1: *component-based approach to load modelling.*

The main advantage of the component-based approach is that system measurements are not required, making this method relatively cheap and easy to implement. Once the characteristics of all relevant individual load components are known, only further information required to form load models at different buses are their load mixes. In this way, the approach may be used to predict the changes in bus load characteristics with changes in load inventory and load mix. A disadvantage to this modelling approach is that information about the load class mix has to be known. This information is often hard to collect, as it requires detailed statistics of energy by end-use. Also, load class mix is expected to change depending on the time of day (in the short term) and by season (in the longer term), which is also a challenge faced in the measurement based approach. However, with Governments and commercial companies increasingly collecting data on consumer trends and lifestyle habits, the required data is becoming more accurate and readily available. An example of this is the 'whatif' tool [14], commissioned by Department for Environment Food and Rural Affairs (DEFRA) in collaboration with several market research companies. This tool provides detailed statistics on the present and predicted future energy consumption by load type and energy end-use in the UK domestic and commercial sectors.

In order to facilitate the component-based approach to load modelling, research in the late 1970s to early 1980s focussed on investigating the characteristics of loads commonly found at that time. Much of this research was performed in the original EPRI projects, with references [15] and [16] providing exponential models of typical loads. Table 1.1 presents a selection of the developed exponential load models from [9] , [15], [17] and [18], as summarised in

Table 1.1: *Exponential model coefficients of typical load components, [19].*

Component	Power factor	np	nq
Water heater	1.0	2.0	0
Oven	1.0	2.0	0
Deep frier	1.0	2.0	0
Clothes washer	0.65	0.08	1.6
Refrigerator	0.8	0.77	2.5
Television	0.8	2.0	5.1
Incandescent lights	1.0	1.55	0
Fluorescent lamp	0.9	0.96	7.4
Industrial motors	0.88	0.07	0.5
Fan motors	0.87	0.08	1.6
Air conditioner:			
- 3-phase	0.9	0.088	2.5
- 1-phase	0.96	0.202	2.3
- Window type	0.82	0.468	2.5

[19]. Some other results for polynomial load models are found in literature ([20] and [21]), but in essence they are just repeating the exponential models from Table 1.1, which is a compilation of most commonly used load models. The EPRI work represents the last major review of component-based load models, with the exception of [22] in 1998, where some further component-based models are presented.

An IEEE task force on load modelling was established in the early 1990s. This task force published, among others, three key papers on load modelling. The first paper in this series, [3], published in 1993, summarises the state-of-the-art in static and dynamic load modelling. The second paper, [23], published in 1995, gives a bibliography of previous load modelling work and load models. This paper discusses how static load models of typical load components are often derived from measurements, but does not present any component-based load models. The third paper, [4], also published in 1995, recommends load models that should be used for dynamic performance analysis, and also gives examples of static load models for load components. The presented models of these components are the same as in Table 1.1, which also illustrates lack of work in identifying accurate load models for various load types. A more recent summary of current load modelling was published in a literature review in 2006, [24], where, over 100 load modelling references are listed, although none, with the exception of [22], provided updated component-based load models since the 1980s.

In many conventional load flow studies, constant power load model is typically used as it is considered a "worst case model", ([2], [22], [25] and [26]), in terms of load flow. This is because if system voltage reduces this load type will not reduce its demand, as is the case for both constant current and constant impedance models. However, characteristics of even the limited number of loads in existing literature are different from constant power load type.

1.2 On the need for new load component models

The major engineering challenges of the future will more than ever before be concerned with the distribution system (i.e. medium and low voltage networks). This is due to an increased amount of distributed generation, increased demand and the need to operate these networks actively to improve both performance and efficiency. New concepts of end-use of electricity, such as demand side management, are now being seriously considered. All these challenges require that used load models are accurate, flexible and versatile, and component-based approach to load modelling is well suited to meet these (present and future) needs.

From the review of relevant literature and previous discussion, it is clear that the majority of component-based load models were developed over twenty years ago. These early models may not be able to accurately model modern loads, even if they are of the same type. The inadequacy of using older load component models is clearly expressed in [27], where a proposal for a new EPRI project to update the component-based load models in residential, industrial and commercial load sectors is formulated. Reference [28] also expresses the need to update these old models. A good example of the need for updating is television load, which, according to [16], should be represented as a constant impedance load, see Table 1.1. Reference [16] was published in 1982, and at this time the representation of this load type was indeed correct, but research presented in this thesis clearly shows that modern televisions are constant active power loads. This is only one example, highlighting the fact that previously developed load component models cannot be used to represent/model modern load.

Since the last major review of load models, there have also been considerable changes in the load inventory, [24]. The most significant changes include increased numbers and new types of non-linear loads. A load is classed as non-linear if it draws a non-sinusoidal current from the supply system. Examples of these loads include devices such as adjustable speed drives (commonly used in the industrial and commercial load sectors), personal computers, monitors, televisions and other consumer electronic equipment. Other non-linear loads, such as compact fluorescent lighting, have increased significantly in the past few years, and are expected to completely replace traditional incandescent lighting in the next few years. As concerns about energy efficiency grow, a new generation of single-phase drive-controlled motors is expected to emerge. These are also non-linear loads. There has been little recently published work on how these new types of loads should be represented in power system studies. Accordingly, the majority of load models used in traditional power system studies are becoming outdated, as they are unable to accurately represent power demand characteristics of present and future loads. Many examples were found where older component-based load models are being used as a matter of default, with no further consideration. For example, [2] (2007) and [29] (2004). This is because many standard text books that present load models (mainly in exponential form) have not been updated with new characteristics, which further highlights the general uncertainty

of what these characteristics may be.

Finally, up until now the harmonic characteristics of non-linear loads have been considered as a completely separate area to standard power system (i.e. load flow) analysis, and therefore existing/previous load models did not consider them. However, as system voltage distortion increases due to the presence of these non-linear loads, this assumption should be re-evaluated. This thesis shows that distortion of the system voltage will have significant effect on the power demand characteristics of certain non-linear loads, and that the harmonic content associated with individual load types has led to the creation of several new sub-types of load due to harmonic legislation introduced in 2001, [30].

Therefore, in order to accurately predict both active and non-active power demand characteristics of aggregate modern power system loads in different load sectors (e.g. residential, commercial or industrial), existing component load models should be updated and new models developed.

1.3 Aims of this thesis

The two main aims of this thesis are to update existing static component-based load models and develop new load models where necessary. In order to achieve these aims, a full review of typical types and sub-types of modern system load components is required. The updated and newly developed load models should be able to accurately represent the active and reactive power demand characteristics of both individual and a aggregate of same type/sub-type load. Where possible, the developed models should also be compared to existing load models. As many of the loads to be modelled are non-linear, an additional aim of the thesis is to accurately represent the typical harmonic characteristics of these loads. This is a significant extension to the previous component-based load models, which have traditionally only considered active and reactive power demand of each load component. This extension is deemed necessary for several important reasons. Firstly, recently introduced EU (European Union) harmonic legislation in 2001, [30], has led to significant changes in the harmonic characteristics of many common non-linear loads used in domestic and commercial sectors. This is because many non-linear loads found in these sectors include some form of power factor correction (PFC) to reduce their harmonic emissions. Secondly, harmonic legislation has also indirectly affected their active and reactive power characteristics, as the inclusion of PFC circuits and techniques was required to satisfy specific harmonic limits. From the review of available literature, the implications (present and future) of harmonic legislation have not been fully investigated with regards to power system load flow and harmonic studies. Active/reactive power demand and harmonic characteristics of modern power system loads are not independent of each other, and accordingly must both be considered in representative load models. Finally, distortion of

the supply system voltage due to increased numbers of non-linear loads will also affect power demand characteristics of modern aggregate power system loads, which has not been previously considered in existing literature.

This thesis further aims to show how the developed generic load models can be used to form present and expected future aggregate loads. To illustrate this the effects of applied load models on a typical distribution system are compared in this thesis for both developed load models and standard/existing load models. This comparison highlights the importance of having accurate load models for both design and operation of distribution systems. The harmonic characteristics of present and expected future aggregate load are also discussed in line with the likely effects of increased numbers of non-linear load on typical distribution system load buses, as well as the system-load interaction when non-linear loads is a significant part of the aggregate load.

The final and ultimate aim of this thesis is to deliver an updated and extended library of comprehensive load models of loads found in modern power supply systems. The developed load models from this library should be accurate and flexible, i.e., suitable for use in either standard load flow analysis or more detailed harmonic investigations, or a combination of the two. By answering this requirement, the thesis will provide a versatile load modelling tool, which can be used in a wide range of further applications and not just specifically load flow analysis.

1.4 Structure of the thesis

The thesis is divided into seven chapters, four of which are dedicated to the development of models of specific types of power system load. The following types of load commonly found in the supply system are considered in this thesis: three-phase directly connected and drive-controlled motors, single-phase directly connected and drive-controlled motors, power electronic loads and lighting loads. The aim of each load modelling chapter is to present full, equivalent circuit and generic analytical load models from which standard exponential and polynomial interpretations are derived. The following procedure is used to develop these load models:

1. For each considered load type, common sub-types are identified.
2. For each relevant load type/sub-type typical circuit topologies are established.
3. Full/detailed simulation circuit models are then developed for each load type/sub-type based on their typical circuit topologies.
4. Developed full model(s) are validated against either measured data, or against existing model of the corresponding load type available/built in a different software.

5. Full circuit model(s) are then converted to an equivalent circuit model(s), which is/are also verified and validated.
6. Equivalent circuit model(s) are then converted into analytical forms and again verified.
7. Existing literature is used in combination with harmonic legislation to identify and quantify the typical per-unit values of key load type/sub-type parameters.
8. This information is then used to establish generic analytical model(s), able to accurately represent same type/sub-type aggregate loads.
9. Polynomial and exponential interpretations of developed generic analytical models are derived next.
10. Generic models are then used to form mixed-type aggregate loads representing different load sectors (residential, commercial etc.)

The proposed generic models are given in per-unit (pu) form, and are able to represent the power and harmonic characteristics of an aggregate same-type (or where relevant sub-type) of load. Two types of aggregate load models are developed. The first are in exponential and polynomial form, and therefore may be used directly in standard power system load flow studies. The second type is presented in analytical and equivalent circuit forms, and is able to represent all harmonic, active and non-active power characteristics of the considered load types/sub-types. The developed polynomial and exponential modes in each load modelling chapter are also compared with previously published load models, (where available).

After the models of each type/sub-type of load have been developed, they are used to form aggregate mixed-type loads, representing current and expected future load mixes. The power demand and harmonic characteristics of these aggregate loads are discussed and network models are used to investigate their effect on load flow analysis. These results are also compared with those of related existing load models. The effects of estimated present and future load mixes on voltage distortion at a typical load bus are also considered as a part of general discussion of system-load interactions.

It should be noted that the load models developed in this thesis do not consider the effect of variations in supplied system frequency. This is because expected steady state variations in system frequency will be very small and therefore will have no significant influence. Furthermore, [22] has shown that non-linear loads are essentially frequency-independent.

1.5 Thesis outline

As stated previously, this thesis consists of seven chapters. A brief summary of each chapter is outlined below.

Chapter 1

This is an introductory chapter, reviewing previous work in the area of load modelling, with particular attention on component-based load modelling. It also outlines the general need and motivation for new work in this area.

Chapter 2

This chapter investigates three-phase motor loads. Two general types of these loads are considered: three-phase motors directly connected to the supply system, and three-phase motors connected/controlled via adjustable speed drive (ASD). It is concluded that directly connected motors should be split in two following sub-types: lower-power motors and higher-power motors. It is further shown that the change in active and reactive power demand of lower-power motors with change in system voltage (their P-V and Q-V characteristics) are dependent on the type of mechanical load the motor is driving. The P-V and Q-V characteristics of higher-power directly connected motors, however, are independent of motor mechanical loading condition. The P-V characteristics of ASDs will depend on the type of drive-control, rated power of the ASD (lower or higher) and, in certain cases, the type of mechanical load of controlled motor. The non-active power (N-V), and harmonic characteristics of these loads will depend on the type of mechanical load, the conduction mode of the three-phase rectifier in the ASD, the value of dc link parameters and, to a certain extent, on the value of the local system impedance. It is further shown that current harmonic legislation will not have significant influence on the design of these load types. Full circuit, equivalent circuit, analytical, exponential and polynomial load models are all developed for the representation of this load type. *(Published papers from this research: [31], [32] and [33])*

Chapter 3

This chapter considers directly connected single-phase induction motors and single-phase drive-controlled (SASD) motors. It is shown that, from a static load modelling perspective, there are two main types of single-phase directly connected induction motors. The active and reactive power demand characteristics of these two types of load are investigated, and it is concluded that their P-V characteristics will depend on the type of motor mechanical

loading and the type of drive-control, while their Q-V characteristics will not. Typical types of single-phase drive-controlled motors are identified and investigated in detail. Here, it is found that, although not common at present, these load types are expected to increase significantly in the near future. It is shown that harmonic legislation will have a significant effect on the non-active and harmonic characteristics of these loads, as SASD of rated power greater than approximately 400W will require power factor correction. Accordingly, their N-V and harmonic characteristics will depend on rated active power, type of applied mechanical loading and value of dc link components. It is also shown that displacement power factor of lower-power SASDs will be affected by the presence of distortions in supply system voltage. In order to acknowledge this, the thesis recognised two sub-types of SASD load: those without power factor correction (lower-power SASDs) and those with (higher-power SASDs). Full circuit, equivalent circuit, analytical, exponential and polynomial load models are developed for each identified type and sub-type of this load. *(Published paper from this research: [34])*

Chapter 4

This chapter investigates power electronic loads, which are commonly found in domestic and commercial load sectors. As the vast majority of these loads will contain switch-mode power supplies (SMPS), the typical topologies and configurations of SMPS are considered and discussed. The effects of harmonic legislation on these loads is also considered, and it is concluded that due to this legislation there will be three distinctive sub-types of electronic load. The P-V characteristics of each load sub-type are similar, and can be represented by a constant active power load. However, the non-active and harmonic characteristics of each load sub-type differ significantly. This has implications for both load flow and harmonic analysis, as these loads were previously considered to be all of the same type. It is also found that the displacement power factors of these loads will be affected by the presence of distortion in system voltage. Full circuit, equivalent circuit, analytical, exponential and polynomial load models of the three sub-types of electronic loads are developed. *(Published papers from this research: [35], [36])*

Chapter 5

This chapter considers lighting loads. It focuses on compact fluorescent lighting (CFL), as this type of lighting is expected to replace incandescent lighting loads in the near future. The typical topologies of the ballast used to control these types of fluorescent light sources are considered. It is found that older type magnetic ballast, on which existing fluorescent lighting load models are based, are now obsolete. Furthermore, it is found that the present models of compact fluorescent tubes are also somewhat outdated. Accordingly, a new compact fluorescent tube

model is developed from measurements of modern compact fluorescent lights. It is shown that harmonic legislation will have a significant effect on the design, and therefore active, non-active and harmonic characteristics of this load. It is also found that the displacement power factor of this load will change significantly if there are distortions in system voltage. Once again, full circuit, equivalent circuit, analytical, exponential and polynomial load models are developed and presented for CFL lighting load. *(Published paper from this research: [37])*

Chapter 6

This chapter uses previously developed generic analytical models of considered individual load types and sub-types (chapters 2-5) to form aggregate loads. Typical present and expected future load mixes are established from available statistics, to enable load bus aggregates to be formed. In doing so, present and future loads are investigated and discussed, and it is shown that diversity introduced into the aggregate load by different load sub-types (mainly due to new harmonic legislation) will have significant effect on harmonic characteristics of the aggregate load. It is also shown that distortion of the system voltage will affect fundamental reactive power demand of the aggregate loads and, hence, the results of load flow analysis. Aggregate loads formed from proposed models are also compared to aggregate loads formed from existing models, with both applied to a typical distribution network. The load meeting capacity of the network is investigated with the different aggregate loads. Finally, the effect of expected future load mix on the voltage distortion at a typical distribution system bus is also investigated.

Chapter 7

This chapter presents conclusions from the work presented in this thesis, as well as suggestions for further work.

Appendices

Figures and information not included in the main body of the text are presented in the Appendices. A list of publications from the research presented in this thesis can also be found in the Appendix E.1.

1.6 Main contributions of the thesis

The following are main contributions of this thesis:

- Development of new component-based load models, for use in power system load flow

studies and harmonic studies, with respect to following main types and sub-types of the loads found in modern power systems:
- Three-phase directly connected motors
- Three-phase drive-controlled motors
- Single-phase directly connected motors
- Single-phase drive-controlled motors
- Power electronic loads (dc power supplies and SMPS)
- Lighting loads, specifically CFL.

- Development of generic equivalent circuit models and analytical models for above mentioned load types.
- Proposal of new compact fluorescent tube model.
- Investigation into the effects of recent harmonic legislation on the characteristics of modern non-linear loads and typical aggregate power system loads.
- Discussion of the active, reactive and harmonic characteristics of expected future system load and their effect on a typical distribution system.
- The importance of including harmonics in standard power flow analysis.
- Seven published international conference papers.

1.7 Definitions of electrical power quantities used in this thesis

Traditional methods of calculating active, reactive and apparent powers assume sinusoidal currents and supply voltages. This assumption, however, is not valid when considering non-linear loads. For more than a century, the definition of reactive power for non-sinusoidal supply conditions has been a contentious subject. More recently, there has been much discussion on the practical definitions of power quantities under non-sinusoidal supply conditions. This has led to the development of an IEEE standard, [38]. Definitions from this IEEE standard will be used for the representation of power quantities in non-sinusoidal situations in this thesis, (Table 1.2).

In these definitions, the displacement power factor, PF_1, is typically used when considering capacitors for reactive power compensation [39]. Thus, when considering the reactive power consumption of non-linear loads, fundamental reactive power, Q_1, is taken as being analogous to Q in linear loads. Accordingly, developed exponential and polynomial models represent Q_1 characteristics of non-linear load. References [39], [40] and [41] provide detailed discussions of these definitions.

1.8 System impedance

In the work presented in this thesis typical values of system impedance are often required. The value of system impedance will vary depending on the considered point in the supply system network and, accordingly, no single value of system impedance may be defined for all points. However, as much of the load considered in the thesis will be found in the domestic sector, the value of system impedance may be defined for typical UK domestics networks. From extensive review of European networks, reference [42] predicts that 90% of UK residential consumers will have supply impedance equal to or less than R = 0.25Ω, X=0.23Ω and that 98% of customers will have supply impedance equal to or less than R = 0.46Ω, X=0.45Ω. Therefore in this thesis Z = (0.25 + j0.23)Ω is taken as a nominal system impedance; Z = (0.46 + j0.45)Ω is taken as a maximum expected system impedance, and Z = (0.12 + j0.11)Ω is the minimum expected system impedance. The minimum value of impedance is an estimate, as no value was stated in [42].

Table 1.2: *Summary of quantities and indicators for non-sinusoidal waveforms, [38].*

Quantity / indicator	Fundamental and all harmonics	Fundamental only	Harmonics
Apparent Power (VA)	$S = V \cdot I$ $S^2 = S_1^2 + S_N^2$	$S_1 = V_1 \cdot I_1$ $S_1^2 = P_1^2 + Q_1^2$	$S_N^2 = D_i^2 + D_v^2 + S_H^2$ $S_H^2 = (V_H \cdot I_H)^2$
Active Power (W)	$P = \frac{1}{T}\int_0^T v \cdot i.dt$	$P_1 = V_1 \cdot I_1 cos\theta_1$	$P_H = \sum_{h \neq 1} V_h \cdot I_h \cdot \cos\theta_h$
Reactive and Nonactive Power (VAr)	$N = \sqrt{(S^2 - P^2)}$	$Q_1 = V_1 \cdot I_1 \sin\theta_1$	$D_i = V_1 \cdot I_H$ $D_v = V_H \cdot I_1$
Line utilisation or power factor	$PF = \frac{P}{S}$	$PF_1 = \frac{P_1}{S_1} = \cos\theta_1$	$PF_d = \frac{1}{\sqrt{(1+THD_i^2)}}$*, $PF_d = \frac{PF_1}{PF}$ $THD_x = \frac{X_H}{X_1}$

* for sinusoidal voltage.

Where: V and I are rms voltage and current, v and i are instantaneous values of voltage and current, PF, PF_1 and PF_d are true, displacement and distortion power factors respectively, THD is total harmonic distortion. Subscript 1 defines fundamental component, h defines the harmonic order, H is the sum of all harmonics components without the fundamental and T is the time of one cycle at the fundamental frequency

Chapter 2
Three-phase directly connected and drive-controlled induction motors

2.1 Introduction

For more than a century, induction motors have been known as the workhorse of the industry, providing a cheap and robust solution for efficient conversion of electrical into mechanical energy. The vast majority of motors are low voltage motors, as high voltage motors are rare, and used in (very) high power applications, greater than 500kW. High voltage motors are usually custom designed and should be modelled as individual loads, depending on their specifications. Therefore, only low voltage motors are considered in this thesis. It is estimated that electric motors in EU consumed 860 Twh of power in 2005, making up roughly 53% of the total power consumption for that year, with three-phase induction motors representing over 90% of this energy consumption [43].

Three-phase induction motors have proved popular, due to their simple construction, high efficiency (up to 95%), low electromagnetic interference, ability to be directly started from the supply system and low cost per kW when compared with other motor technologies. However, three-phase induction machines directly connected to the supply system exhibit high starting currents, low power factors and difficult or very limited speed/torque control. To overcome these disadvantages, adjustable speed drives (ASDs) are used in applications in which more sophisticated or optimal control of induction motors is required. Besides significantly improved speed and torque control, ASDs also offer energy savings in part-load applications (20-30%, [44]), reduction of noise, mechanical and thermal stresses, remote control and communication, low maintenance and automated diagnostic. These benefits, connected with the mass-production and constantly decreasing prices, resulted in a wide use of ASDs in many industrial and other applications. Modern ASDs allow induction motors to achieve the same torque/speed performance as that of dc motors, but with increased reliability. It is estimated that of all connected induction motors, the number of ASD-controlled induction motors varies between 5% (low-power applications) and 20% (high-power applications), [45], with these numbers expected to increase significantly over the next years. Table 2.1 shows the breakdown of the European motor market in 2005 for the EU-15 countries. This table shows that the vast majority of motors are in the 0.75 - 7.5 kW power range, with the higher power motors less

common. There was no available data for motors of rated power greater than 200kW. Table 2.2 lists the typical number of magnetic poles used in induction motors, showing motors with two pole pairs as dominant.

Table 2.1: *Three-phase induction motor market data for EU-15 countries in 2005, [43].*

Power Range kW	Number of units millions	Market Share units	Total Capacity GW	Market Share Capacity
$0.75 - 7.5$	7.2	79.1%	22.5	28.2%
$7.5 - 37$	1.5	16.5%	30.0	37.6%
$37 - 75$	0.3	3.3%	15.6	19.6%
$75 - 200$	0.1	1.1%	11.6	14.6%
Total	9.1	100%	79.7	100%

Table 2.2: *Comparison of motor pole pairs and market share.*

Motor Pole Pairs	Market share (%)
1	25
2	60
3	11
4	4

Although there has been much previous work into dynamic representation of three-phase directly connected motors for transient analysis, there has been less work on deriving analytical representations of these loads for steady state analysis, i.e. exponential and polynomial motor load models. Table 2.3 presents only a very few previously derived exponential models of directly connected three-phase motors found after the review of relevant literature. This previous work suggests that the variation of motor active power with system voltage is relatively independent of the application in which the motor is used, while the change in reactive power with system voltage is dependent on motor application.

Table 2.3: *Existing exponential load model coefficients of directly connected three-phase motors.*

Motor Type	Power factor	Exponential model coefficients		Source
		n_p	n_q	
Small Industrial	not specified	0.1	0.6	[25]
Large Industrial	0.88	-0.01 to 0.07	0.5	[25],[29],[15],[19]
Pump/Fan	0.87	0.08	1.6	[25],[29],[15],[19]
3-phase air con.	0.90	0.088	2.5	[19]

Due to the non-linear operation and additional electronic/control circuits, there are certain

differences in steady state electrical and operational characteristics between directly connected and ASD-controlled motors, of which harmonic emission and alteration of active/reactive power flows are the most prominent. There has been relatively little research into steady state load models of ASDs, with only one reference found to present a load model of ASDs, Table 2.4.

Table 2.4: *Existing load model coefficients of ASDs, [22].*

Loading	PF_{nom}	Exponential Model		Polynomial Model					
		np	nq	Z_p	I_p	P_p	Z_q	I_q	P_q
ASD 1	0.79	1.47	1.34	0.43	0.61	-0.05	-1.21	3.47	-1.26
ASD 2	0.79	2.12	1.98	3.19	-3.84	1.65	1.09	-0.18	0.09

This chapter investigates the P-V and Q-V/N-V characteristics of typical types and configurations of three-phase directly connected and drive-controlled induction motors. The effects of the type of applied motor mechanical loading condition are considered, as well as the effect of changing key motor and drive parameters. Detailed transient motor and drive models are developed from existing theory, in order to perform the required analysis.

The results of the analysis performed on directly connected motors are used to develop corresponding polynomial and exponential models. It is shown that while exponential and polynomial models may be used to represent active power demand characteristics of ASDs, care should be taken when using them to represent fundamental reactive power characteristics. This is because non-active power characteristics of these loads are dependent on the value of key drive components and, to a lesser extent, the local system impedance where the drive is connected. By changing the values of these components, non-active power demand characteristics of these loads will be significantly altered.

In order to fully represent ASD non-active power demand characteristics, an equivalent circuit model of the ASD is developed and verified. This equivalent circuit models is then converted into analytical form. The resulting analytical model is able to represent the two distinctive operating modes of ASDs, including all active and non-active power demand and harmonic characteristics of these loads. The analytical model is then generalised and subdivided, based on the type and rated power of the ASD to be represented. In this way, the developed models are able to represent any typical load mix of ASDs, with only required information being the percentage contribution of each type of ASD to the total power. Polynomial and exponential interpretations of proposed generic analytical load models are also presented.

2.1.1 Motor mechanical loading

Although there is a wide diversity in mechanical characteristics of loads driven by induction motors, it is possible to classify mechanical loads into four general types: constant torque, linear torque, quadratic torque and constant mechanical power, as shown in Figure 2.1. Each of these four general mechanical load types are discussed briefly, with Table 2.5 giving the associated torque equations, [46].

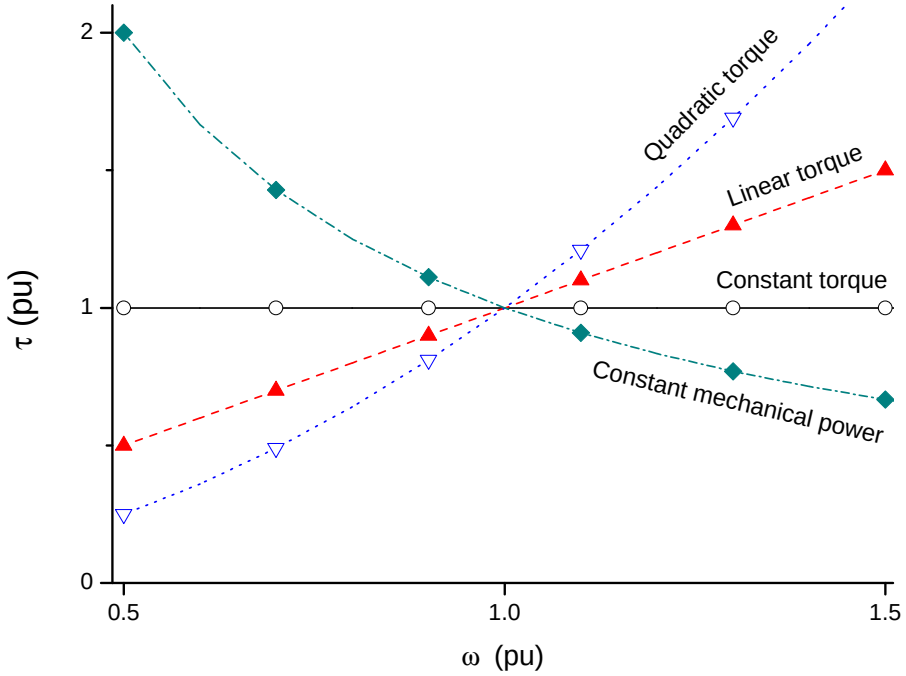


Figure 2.1: *Four general types of mechanical loads.*

Table 2.5: *Four general types of motor mechanical load, [46].*

Mechanical Load Type	Torque Equation
constant torque	τ_{load} = constant
linear torque	$\tau_{load} = \frac{\omega}{\omega_{nom}}$
quadratic torque	$\tau_{load} = \frac{\omega^2}{\omega_{nom}}$
constant mechanical power	$\tau_{load} = \frac{\omega_{nom}}{\omega}$
Where: ω_{nom} is nominal motor speed and ω is actual motor rotational speed.	

2.1.1.1 Constant torque mechanical loads

Mechanical loads that fall into this category are loads in which torque demand is not a function of motor mechanical speed. For this load, the demanded mechanical power will change linearly with the motor mechanical speed. Some typical examples of these types of loads ([47]) include: conveyors, traction drives, positive displacement pumps and reciprocating and rotary

compressors.

2.1.1.2 Linear and quadratic torque loads

These loads are sometimes generally referred to as variable torque loads, for which load torque requirement varies either as a linear or quadratic function of the changes in motor speed. These loads will draw less power when motor speed is reduced and more power as motor speed increases. Typical examples of these mechanical load types include: axial and centrifugal fans, blowers and compressors.

2.1.1.3 Constant mechanical power loads

Constant mechanical power loads will draw constant mechanical power independent of the motor rotor speed, with load torque changing in inverse proportion to the motor speed. This mechanical load type is also sometimes referred to as constant horsepower load. Some examples of these load types include: grinders, winders, lathes and tension drives.

2.2 Typical three-phase motor drives

The dominant type of ASDs in the range from a few kW up to several MW is the pulse-width modulation (PWM) controlled voltage source inverter (VSI). In essence, the PWM ASD is a converter, comprising of a bridge rectifier, a dc (direct current) link filter, an inverter, and additional control, protection and measurement circuits. Figure 2.2 shows a typical configuration of a three-phase PWM ASD. It should be noted that there are other types of ASDs that use different 'front-ends' to the three-phase bridge rectifier considered in this work, however their percentage contribution to total ASD load compared to that of ASDs with three-phase bridge rectifiers is small and accordingly they are not considered in this thesis.

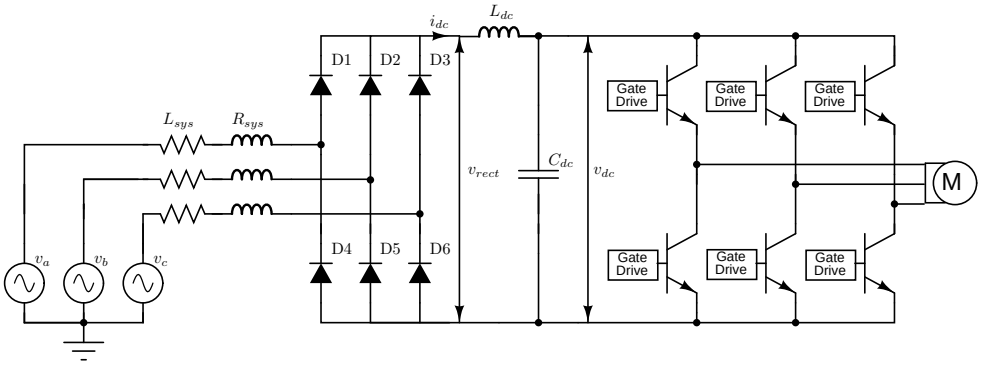


Figure 2.2: *A typical three-phase PWM adjustable speed drive.*

Speed and/or torque regulation of an ASD-controlled induction motor is achieved by the use

of electronic and control circuits, which convert fixed frequency/magnitude input ac (alternate current) supply voltage into a variable (i.e. adjustable) frequency/magnitude output voltage at the motor terminals. This conversion is normally performed in three stages. Firstly, the ac supply voltage is rectified by a passive front-end three-phase rectifier, usually a full-bridge diode or thyristor rectifier. Next, the rectifier voltage is smoothed to a dc voltage, by a dc link filter circuit, consisting of an inductance, L_{dc}, and capacitance, C_{dc}. Finally, the three-phase switching transistor/IGBT inverter converts the dc link voltage to an ac voltage of desired frequency and magnitude. Depending on the control strategy and switching function applied to the inverter, different types of ASDs can be established. In this thesis, four types are considered: open-loop PWM V-Hz, closed-loop PWM V-Hz, direct torque controlled and field oriented ASD. Of these, the V-Hz control technique is currently the most common type of drive control.

2.2.1 Rectifier circuit

The passive front-end three-phase diode bridge rectifier is the industry standard circuit for ac to dc voltage conversion. The operation of the three-phase bridge rectifier may be split into two distinctive modes: a) continuous current conduction mode, where the dc link filter inductor current never falls to zero, and b) discontinuous current conduction mode, where it does. The value of the dc link filter L_{dc} relative to the rated power of the ASD will dictate the mode of operation of the rectifier. Each of these two modes of operation are discussed below.

2.2.1.1 Discontinuous current conduction mode

The diodes in the three-phase rectifier will rectify the input three-phase system voltage to produce an ac voltage with a dc offset, v_{rect}. This voltage follows the envelope of the maximum system line voltages, as shown in Figure 2.3(a). When v_{dc} is less than v_{rect}, current will be drawn from the supply system, and v_{dc} will increase as the dc link capacitor is charged, (conduction subinterval). However, due to inductances in the rectifier circuit, L_{dc} and L_{sys}, the capacitor charging current can not instantly increase, and there will be a period where the current supplied to rectifier load, i.e. to the inverter and motor, will still be greater than the charging current supplied by the system. Hence, v_{dc} will continue to decrease for this period. When v_{dc} is greater than v_{rect}, no current will be drawn from the supply system (cut-off subinterval), and the dc link capacitor will discharge through the rectifier load. However, again due to inductance in the conduction path L_{dc}, current can not instantaneously stop flowing when v_{dc} is greater than v_{rect}. Therefore, there is a period prior to the cut-off subinterval where the current is decreasing through L_{dc}, causing v_{dc} to continue to increase until the current through L_{dc} is zero. This charge and discharge process results in the current and voltage waveforms shown in Figure 2.3, which also shows conduction patterns for the diodes in Figure 2.2.

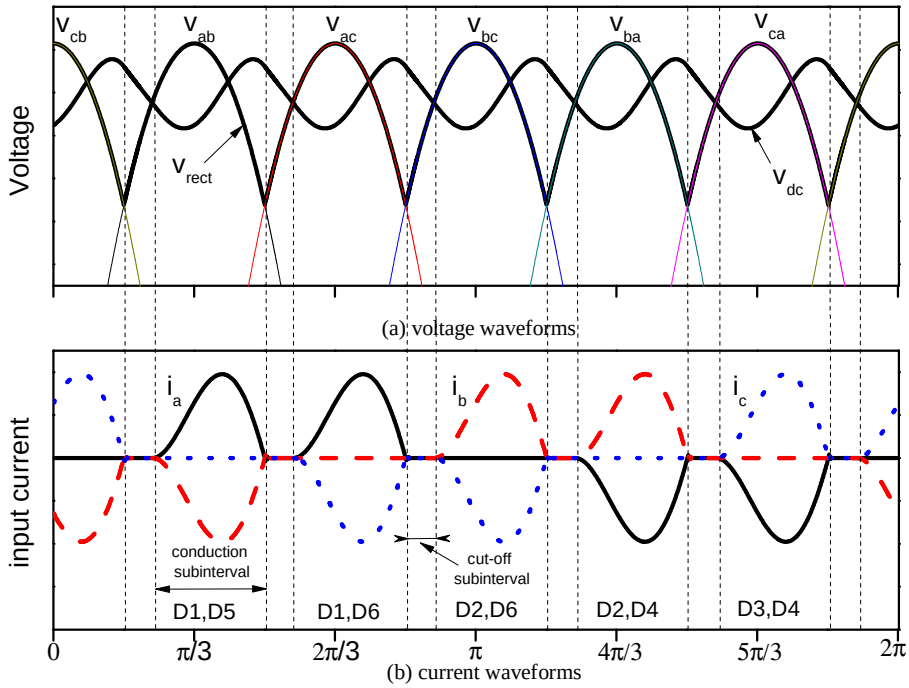
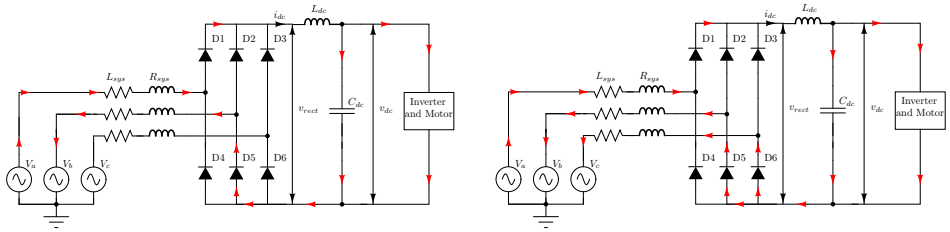


Figure 2.3: *Associated waveforms of three-phase bridge rectifier operating in discontinuous current conduction mode.*

2.2.1.2 Continuous current conduction mode

As previously explained, at the exact point when v_{dc} becomes greater than v_{rect}, current can not instantly stop flowing in the conduction path due to the presence of the inductances, L_{dc} and L_{sys}. In discontinuous conduction mode, the current has time to reduce to zero before the next phase starts to conduct. When a larger value of L_{dc} is used, continuous conduction mode is realised, and the current in the conduction path does not have time to fall to zero before the next phase starts to conduct. This results in a period where two conduction paths exist in the rectifier circuit simultaneously, with three diodes conducting (as one diode is common to both paths, as shown in Figure 2.4(b)). This period is generally referred to as the commutation subinterval and is only seen in continuous mode of operation.



(a) Conduction subinterval (b) Commutation subinterval

Figure 2.4: *Conduction paths of three-phase bridge rectifier during conduction and commutation subintervals.*

Figure 2.5 shows the typical voltage and current waveforms for a three-phase rectifier operating

in continuous current mode, along with the associated diode conduction patterns.

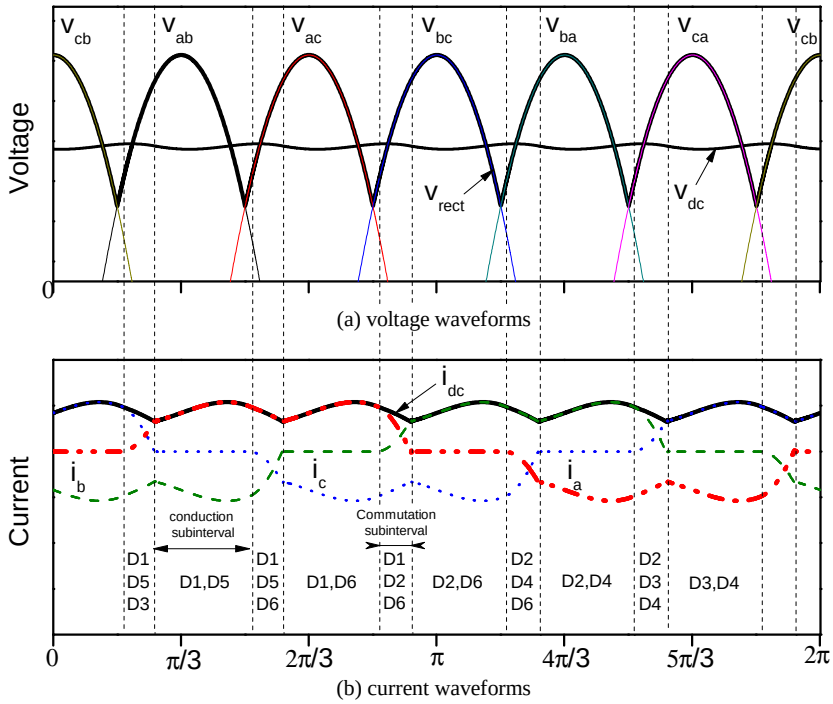


Figure 2.5: *Associated waveforms of three-phase bridge rectifier operating in continuous current conduction mode.*

It can be seen from Figure 2.5 (b) that the dc link current i_{dc} is continuous, following the envelope of the positive input line currents, as dc link current will always flow in the same direction. This current can be divided into the two subintervals: conduction and commutation. The conduction paths for each subinterval are shown in Figure 2.4.

The values of L_{dc} and C_{dc} will both have an effect on whether the rectifier will operate in continuous or discontinuous mode. As discussed previously (Section 2.2.1.1), the greater the value of L_{dc} the longer the time that i_{dc} will take to fall to zero, after v_{dc} exceeds v_{rect}, and the more likely the rectifier will operate in a continuous conduction mode. The value of C_{dc} affects the ac ripple component of v_{dc}, with larger values of C_{dc} leading to a smaller ripple. If the ac voltage ripple component of the dc link voltage is reduced, there will be a shorter conduction sub-interval and therefore more time for the current in the rectifier conduction path to fall to zero before the conduction in the next phase begins. Accordingly, larger values of C_{dc} will tend to 'push' the rectifier towards discontinuous mode operation. It should also be noted that the rectifier operating in continuous current conduction mode supplies dc voltage to the inverter with a much smaller ripple component than the rectifier operating in discontinuous current conduction mode. This is of interest in further discussion of harmonic emissions of this load type in Section 2.5.

2.2.2 Methods of drive control

After the conversion of ac voltage to dc voltage by the three-phase bridge rectifier, the dc voltage is converted back to a fully controllable ac voltage. This ac voltage is produced by means of a three-phase inverter, as previously shown in Figure 2.2. The most common inverter control is the pulse width modulated (PWM) control. The inverter consists of six switching devices, most commonly insulated gate bi-polar transistors (IGBT), but they can also be gate turn off thyristors (GTO), or metal oxide field effect transistors (MOSFETS). These switches are controlled by gate drive pulses derived from comparison of a high frequency triangular wave and a control signal. The phase, frequency and magnitude of this control signal sets the phase, frequency and magnitude of the inverter output voltage. Reference [48] gives a full description of the PWM method of inverter operation. The control signal can be generated by a number of methods. The most common method is a scalar based approach. Much less common at present, but set to increase in the future, are vector based approaches. The block diagram in Figure 2.6, extracted from [49], summarises these control strategies.

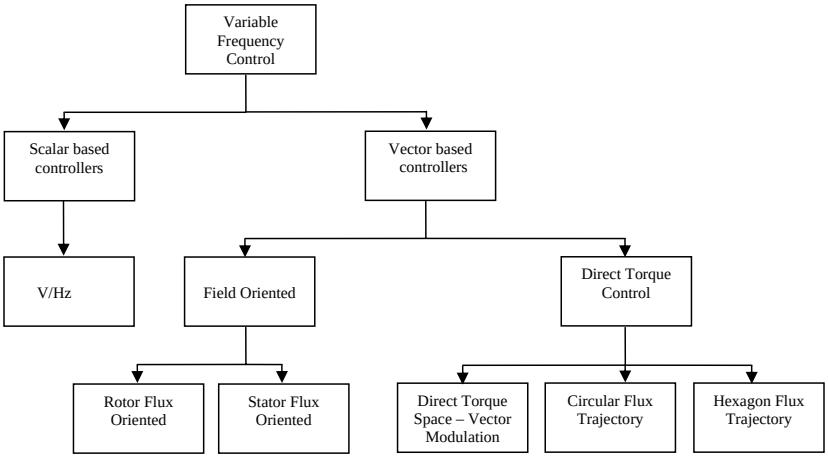


Figure 2.6: *Types of ASD control.*

2.2.2.1 Scalar based control

The scalar based approach is also known as the V/Hz control. Because of its simplicity, it is the most common control used in lower cost drives. V/Hz control operates on the principle that motor speed is proportional to the frequency of the motor stator voltage. In order to avoid motor magnetic saturation, the magnitude of the stator voltage must be changed proportionally to the frequency of the stator voltage. Therefore, by keeping the ratio of magnitude and frequency of the control signal constant, fairly accurate control of motor speed can be achieved. The V/Hz control can be implemented in either open-loop or closed-loop form. Open-loop control is simpler, as no feedback information about the actual motor speed is used in the control circuits. Therefore, the speed of the motor will vary around its set point with changes in machine loading

and system voltage. However, in some applications it is necessary to control the motor speed to be constant. In order to achieve this, closed-loop operation is used, where the actual motor speed is fed-back to the V/Hz controller, which then adjusts the magnitude and frequency of the control voltage to give desired motor speed. Reference [50] gives a detailed description of the theory behind and implementation of V/Hz control.

2.2.2.2 Vector based control

Vector control techniques allow for precise control of induction motors, rivaling the precision control possible with that of dc machines. Vector control technique have only developed relatively recently and require complex hardware and software, hence additional cost. Therefore, vector control is currently less popular than the scalar control methods, and is usually used in high-end applications as a replacement to dc machines. However, as hardware cost reduces, vector control techniques are expected to become more used in the future. Vector control derives its name from the fact that both phase and amplitude of the motor voltage is controlled. There are various techniques of vector control, as outlined previously in Figure 2.6, the most common being field oriented and direct torque control. The theory behind the operation of these controls is given in more detail in [50] and [51].

2.3 Modelling of three-phase directly connected and drive-controlled motors

This section briefly discusses established induction motor and drive models. These models are then built in PSpice software and verified with existing in-built SimuLink models. PSpice software is selected for several reasons. Firstly, it is commonly recognised that PSpice is one of the most powerful modelling softwares on the market, in relation to the accurate representation of power electronic components. Thus, detailed models of the motor drive components can be constructed using this software. Also, PSpice is used for consistency, as all the other device models presented in this thesis are developed in PSpice. Finally, as measurement data was not available to validate the proposed motor and drive models, the developed PSpice models are used to provide validation of the existing SimuLink motor and drive models.

2.3.1 Motor modelling

Although the analysis in this thesis is concerned with steady state characteristics of induction motors, a full transient 4^{th} order model is used during the investigation of motor/drive load models. This is due to two main reasons. Firstly, steady state models can not be used effectively

when motors are controlled by power electronics, i.e. in case of corresponding motor drives. Secondly, using full transient motor models at this stage of the work means that corresponding dynamic motor and drive load models can be developed at a later stage.

There are various methods to represent induction machines analytically. The most complex, and foundation of all models described in this section, is the ABC/abc representation. This representation assumes negligible saturation and losses in the machine core, as well as sinusoidal magnetomotive force (MMF) in the machine air gap. The ABC/abc model is the most diverse of the commonly used motor models, as it can be implemented in situations where the motor is unbalanced, i.e. when input voltages are unbalanced, or in the case of unequal phase impedances. The main disadvantage of this model is its complexity, which makes implementation hard, and results in long simulation times. The reason for this complexity is that many of the machine inductances are represented as functions of rotor speed. Therefore, the machine equations vary in time and are complex to solve. In order to simplify the ABC/abc induction motor model, it can be converted to the two-axis 'dq' reference frame representation. This conversion eliminates the time varying inductances, thus making the dq motor model far less complex than the ABC/abc motor model. The standard dq representation of the three-phase induction motor is given in (2.1) and the corresponding equivalent circuit is shown in Figure 2.7. A detailed description of the derivation of the ABC/abc motor model and its conversion to the dq model motor model can be found in [50] and [52].

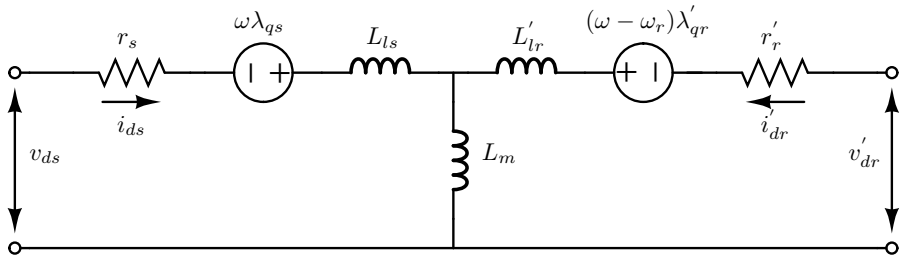
$$\begin{bmatrix} v_{ds} \\ v_{qs} \\ v_{dr}^{'} \\ v_{qr}^{'} \end{bmatrix} = \begin{bmatrix} r_s + L_s\rho & -\omega L_s & L_m\rho & -\omega L_m \\ \omega L_s & r_s + L_s\rho & \omega L_m & L_m\rho \\ L_m\rho & -(\omega - \omega_r)L_m & r_r^{'} + L_r^{'}\rho & -(\omega - \omega_r)L_r^{'} \\ (\omega - \omega_r)L_m & L_m\rho & (\omega - \omega_r)L_r^{'} & r_r^{'} + L_r^{'}\rho \end{bmatrix} = \begin{bmatrix} i_{ds} \\ i_{qs} \\ i_{dr}^{'} \\ i_{qr}^{'} \end{bmatrix} \tag{2.1}$$

where: r_s, L_s, r_r, $L_r^{'}$ are stator and referred rotor resistance and leakage inductance, L_m is the magnetising inductance and i_{ds}, i_{qs}, $i_{dr}^{'}$ and $i_{qr}^{'}$ are stator and referred rotor currents. The stator dq voltages are calculated from abc voltages (v_a, v_b and v_c) using the following expressions:

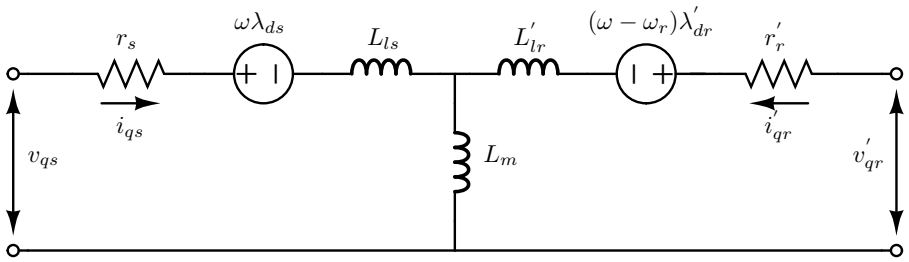
$$v_{qs} = \frac{2}{3}\left[v_a \cos\theta + v_b \cos\left(\theta - \frac{2\pi}{3}\right) + v_c \cos\left(\theta + \frac{2\pi}{3}\right)\right] \tag{2.2}$$

$$v_{ds} = \frac{2}{3}\left[v_a \sin\theta + v_b \sin\left(\theta - \frac{2\pi}{3}\right) + v_c \sin\left(\theta + \frac{2\pi}{3}\right)\right] \tag{2.3}$$

where: θ is phase angle of the reference abc voltage.



(a) d-axis equivalent circuit



(b) q-axis equivalent circuit

Figure 2.7: *Standard dq equivalent circuit for three-phase induction motor, [50].*

The dq motor model is most commonly implemented in one of three reference frames, which are usually selected based on the type of analysis to be performed. The dq model presented in (2.1) is in the arbitrary reference frame, with conversion to the required reference frame performed by setting ω to the desired rotational speed. The three commonly used reference frames, and typical types of analysis for which they are normally applied, are summarised below:

Stationary reference frame $\omega = 0$, this reference frame is best used for the study of transients in the stator, or when the stator is fed by a variable speed drive.

Rotor reference frame $\omega = \omega_r$, this reference frame is used when the rotor variables are of primary interest.

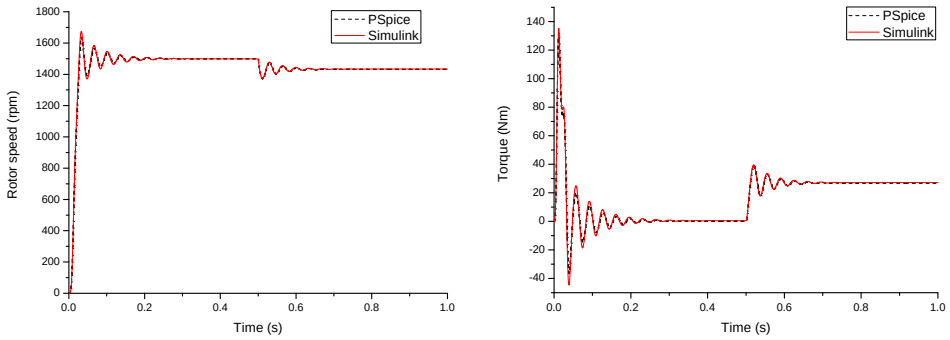
Synchronously rotating reference frame $\omega = \omega_e$, this reference frame can be used to obtain faster simulation results, as larger step sizes can be used, but model detail is lost compared to the other two reference frames.

2.3.2 Development of PSpice directly connected three-phase induction motor model

The stationary reference frame dq motor model was implemented in PSpice software, as motor stator currents are of primary interest in this research, along with the ability to apply drive model to the motor model. As well as the dq motor model, ABC/dq and dq/ABC interfaces

were developed, allowing the analysis of the motor to take place in the ABC reference frame. The PSpice schematics of the developed three-phase motor and interface models are shown in Appendix A.1.

In order to validate the developed PSpice motor model, results of simulations were compared with those produced by the SimuLink motor model, found in the SimPowerSystems block-set [53]. The SimPowerSystems model of the 4kW induction motor was used for the comparison, with the same motor parameters also applied to the PSpice motor model. Figure 2.8 shows the results of this comparison, where both motor models are energised and allowed to reach full rated speed unloaded. Then, rated mechanical loading is applied. The comparison shows that the PSpice and SimuLink models match each other well for rotor speed, rotor mechanical torque and stator input current. This verifies the developed PSpice motor model.



(a) Rotor Speed

(b) Mechanical Torque

(c) Phase a input current

Figure 2.8: *Comparison between Simulink and PSpice results for directly connected 4kW induction motor models.*

2.3.3 Development of PSpice three-phase drive model

The model of the motor drive was implemented in PSpice software, based on the typical ASD, previously shown in Figure 2.2. The full PSpice schematic of the three-phase ASD can be found in Appendix A.2. Initially, a 4kW ASD was built with the following typical drive components:

Rectifier diodes are typical diodes, which are commonly used in drive applications, for

example diode DN4722 [54] in the case of the 4kW ASD.

DC link filter components are standard PSpice inductor and capacitor models, used to represent the dc link filter components L_{dc} and C_{dc}.

Inverter switches are typical IGBT components, for which the ST Microelectronics STGW40nc60v [55] was selected.

Motor is represented as the stationary reference frame dq model of a 4kW induction motor (as described in Section 2.3.1).

2.3.3.1 Validation of PSpice ASD model

In order to validate the developed PSpice ASD model, a SimuLink ASD model was also developed. Both ASD models where built to represent a typical 4kW V/Hz controlled ASD. Nominal values of C_{dc} were selected, (see Section 2.4) and L_{dc} was set to zero. The results of the comparison between these two models are shown in Figure 2.9. The drive-controlled motor is in both cases started initially unloaded until nominal speed is achieved. Subsequently, full rated load is applied to the drive-controlled motor. Both models show good matching to each other. However, the PSpice model draws slightly more input current than the SimuLink model, which is due to additional losses in the PSpice drive model and a more accurate representation of the inverter IGBT switches. This is discussed in more detail in Section 2.3.3.2. The results of the comparisons provide validation for the developed PSpice ASD model.

2.3.3.2 Modelling power electronic switching devices

Full models of the bridge rectifier diodes and IGBT switches based on actual components were used in the PSpice ASD model. The PSpice diode model structure is common and independent of what diode parameters are selected. Therefore, modelling specific diodes has little effect on simulation run time. However, the PSpice model of an IGBT component is complex, leading to a considerable increase in simulation run time when this model is implemented. To investigate whether it is necessary to include the detailed IGBT model for the analysis in this thesis, a comparison was made between the results obtained using the full IGBT model and an ideal switch. The SimuLink ASD model was also included in this comparison, where the SimuLink standard diode and IGBT models were used. The 4kW open-loop V/Hz controlled ASD was implemented for these comparisons. The results are shown in Figure 2.10.

The results of the comparison show that the use of ideal switches leads to a slight under estimation of the drive losses (less than 1%), while the general characteristics of the ASD remain unchanged. For the purposes of this analysis, it is acceptable to represent IGBTs as ideal switches, avoiding long simulation times associated with the use of IGBTs. A similar conclusion is also reached in [56].

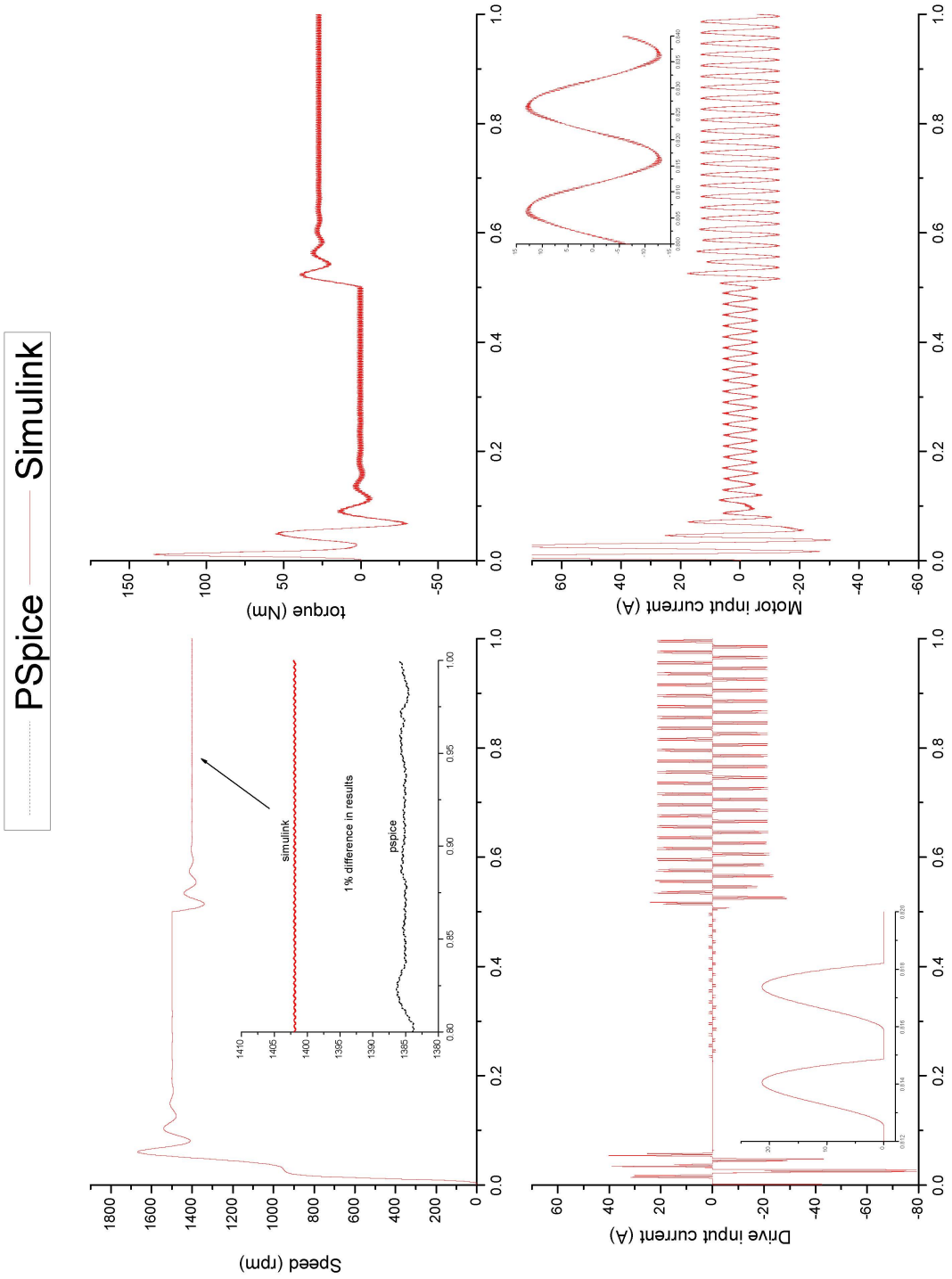


Figure 2.9: *Comparison between Simulink and PSpice results for 4 kW V/Hz open-loop operated ASD models.*

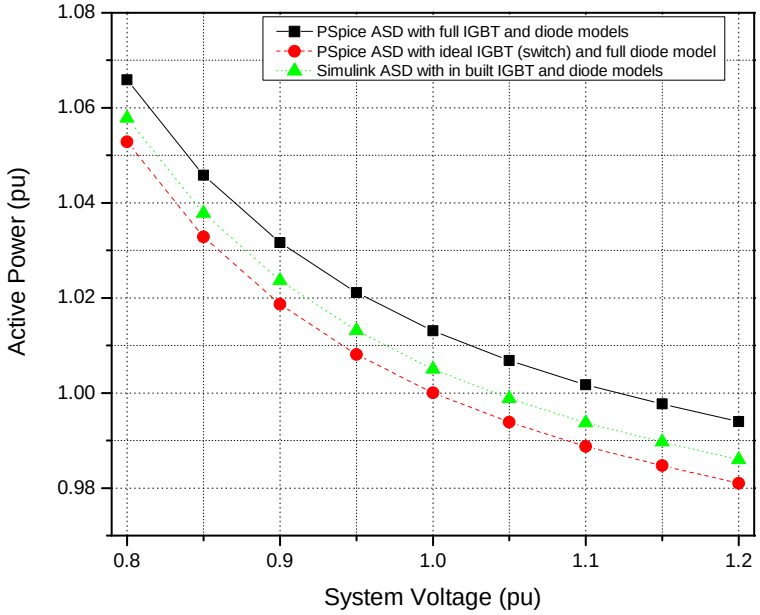


Figure 2.10: *Comparison between different IGBT models.*

2.4 Typical dc link filter component values

The dc link filter circuit of an ASD is typically formed by a relatively large shunt capacitance, C_{dc}, and a relatively small inductance, L_{dc}. The values of the L_{dc} and C_{dc} will depend on the individual application of the ASD, the power rating of the ASD (low-power ASDs often do not have L_{dc}, [57]), the desired mode of operation of the ASD (continuous or discontinuous) and, in some cases, the specific manufacturer of the ASD. The reference [57] identified and presented a range of values for inductive and capacitive dc link reactance $X_{Ldc} = \omega \cdot L_{dc} = 0.002pu - 0.1pu$, with $0.035pu$ being the typical value for the inductive reactance, and $X_{C_{dc}} = \frac{1}{\omega \cdot C_{dc}} = 0.004pu - 0.4pu$, with $0.2pu$ being a typical value for the capacitive reactance. The presented range of typical values of C_{dc} are further confirmed in [58–60], while the typical values of L_{dc} are confirmed in [60]. For the calculation of the per-unit reactance values, the following formulas are used:

$$X_{base} = \frac{V_{phase}}{I_{line}} \tag{2.4}$$

$$X_{pu} = \frac{X_{\Omega}}{X_{base}} \tag{2.5}$$

where: V_{phase} is the rms value of the input ac phase voltage, I_{line} is the rms value of the input ac line current, and X_{base}, X_{pu} and X_{Ω} are base, per-unit and ohmic reactance, respectively.

2.5 Harmonic limits

From the previous discussions of rectifier operation, it is clear that the three-phase rectifier will draw non-sinusoidal current from the supply system that is rich in harmonics. In order to limit the amount of harmonic injected into the supply system, EU-wide harmonic legislation was put in place in 2001. This legislation defines different harmonic limits depending on the rated phase current of the load in question, with the limits split between loads that draw less than 16A per phase (EN 61000-3-2, [30]) and those that draw current greater than 16A per phase (IEC 61000-3-12, [61]) and (IEC 61800-3, [62]). Each of these limits is now discussed.

2.5.1 ASD with nominal input current less than 16A per phase

For a three-phase ASD, maximum input current of 16A per phase at line voltage of 400V (230 V phase) corresponds to a rated power of approximately 11kVA. The harmonic standard relevant in this situation is [30]. This standard states that harmonic limits are not applicable to "professional equipment" of rated power greater than 1kW, with professional equipment being defined as:

> '*Equipment for use in trades, professions, or industries and which is not intended for sale to the general public. The designation shall be specified by the manufacturer, [30]*'

Thus, ASDs with rated power less than 11kVA will be classed as professional equipment, and no specific harmonic limits will be applied to them. This is also confirmed in [63]. It should also be noted that ASD of smaller than 1kW rated power in this work are considered as single-phase adjustable speed drives (SASD), and are discussed in the Chapter 3.

2.5.2 ASDs with nominal input current greater than 16A per phase

If an individual ASD, or a group of ASDs all connected to the same point in a particular installation, exceeds 16A per-phase, then harmonic limits stipulated in [61] apply. These harmonic limits are based on the short-circuit ratio of the supply system at the point of connection of the load(s). Further, if an individual ASD, or an aggregate of ASDs in the same installation, exceeds 75A, [62] applies. This standard stipulates that a harmonic study should be carried out in order to determine the impacts of connecting this load. In both cases, if harmonic reduction is required, it will be performed externally to the ASD. Therefore, the design of individual ASD will not be dictated by harmonic limits, as these harmonic limits will vary dependent on where the ASD is connected to the supply system, and how much ASD/non-linear load is to be connected, or is connected, at that point.

2.5.3 Summary of relevant harmonic limits and their effect on ASD design

From the above discussion, it can be concluded that the design of an individual ASD, specifically the value of L_{dc} in the ASD, will not be dictated by harmonic legislation. This is an important conclusion, as for the other non-linear linear loads considered in this thesis harmonic legislation will have a large influence on their design. Harmonic correction will be applied externally to the ASD, and therefore should be considered on a specific case-by-case basis.

Having stated that the design of a typical ASD is not expected to be determined by the present harmonic legislation, it is still important to make the point that the mode of operation of the rectifier will have a considerable effect on the harmonic content of the rectifier input current. Figure 2.11 shows the current waveforms and associated harmonics for a typical rectifier operating in discontinuous and continuous current conduction modes, (i.e., X_{Ldc} = 0 and X_{Ldc} = 0.035 pu). It can be seen from Figure 2.11 that the rectifier operating in continuous current conduction mode will draw considerably less harmonics from the supply system than the rectifier operating in discontinuous conduction mode. This also means that there will be two distinctive sub-types of ASD loads, those operating in continuous mode and those operating in discontinuous mode.

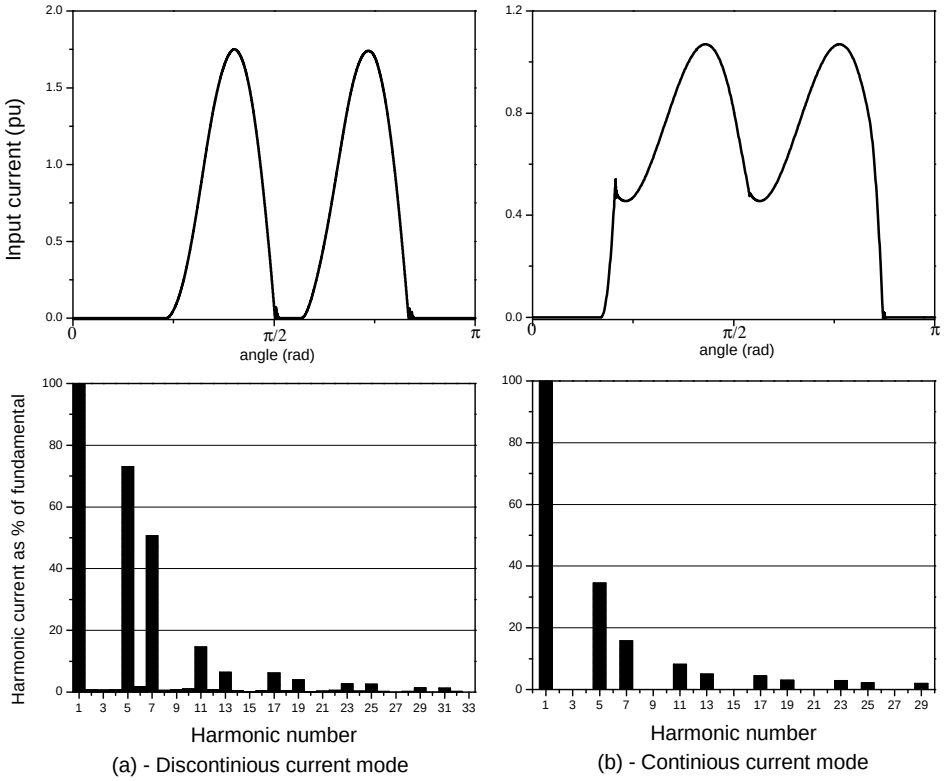


Figure 2.11: *Current waveforms and associated harmonics for a typical ASD operating in (a) discontinuous current operation mode and (b) continuous current operation mode.*

2.6 Active and reactive power demand characteristics of three-phase directly connected induction motors

The characteristics of directly connected motors of different rated active power are now analysed, followed by an investigation of the effect of different motor mechanical loading conditions. The different types of mechanical loading conditions, corresponding to motors used in different applications, are discussed in Section 2.1.1. From these studies, polynomial and exponential load models are developed and compared to existing models.

2.6.1 Per-unit comparison of motors of different rated power

As presented in the introduction of this chapter, the vast majority of directly connected three-phase motors will be low voltage motors with rated power from around 1 kW to 200 kW. Accordingly, Simulink in-built motor models where used to investigate the change in active and reactive power consumption with change in system voltage for motors with rated mechanical powers of 4 kW, 7 kW, 15 kW, 37 kW, 75 kW and 160 kW. These motors are loaded with constant torque mechanical load for this stage of the analysis. The results are presented in per unit (pu), using the following base powers:

$$P_{base} = P_{nom} \tag{2.6}$$

$$Q_{base} = \tan(\cos^{-1}(PF_{nom})) \cdot P_{nom} \tag{2.7}$$

Where: P_{nom} is the motor rated electrical active power, i.e. nominal active power drawn by motor when loaded with rated mechanical load and operated at nominal voltage, PF_{nom} is the motor nominal power factor, i.e., nameplate power factor.

2.6.1.1 Active Power

The analysis in Figure 2.12 shows that the rating of a particular motor only has a small effect on its active power demand characteristics. Figure 2.12 also shows a best fit of these results (see Section 2.7.1), which indicates that the difference between motor per unit active power is always less than $\pm 1\%$ for all investigated motors, even at the ends of considered voltage range. The results show two rough groupings of motor P-V characteristics: those with rated powers below 15 kW, and those above. This is due to motor losses represented by motor efficiency in Figure 2.13. It can be seen that lower power motors are significantly less efficient than higher power motors (due to different design). Also, the efficiency-voltage, $\eta - V$, characteristics of higher power motors are more flat, showing slight reduction only at lower values of system voltage. However, as motor power reduces, correspondingly $\eta - V$ characteristics become

more sensitive, with motor efficiency reducing rapidly at lower values of system voltage. Accordingly, the difference between P-V characteristics of lower and higher power motors is the most pronounced at lower values of system voltage.

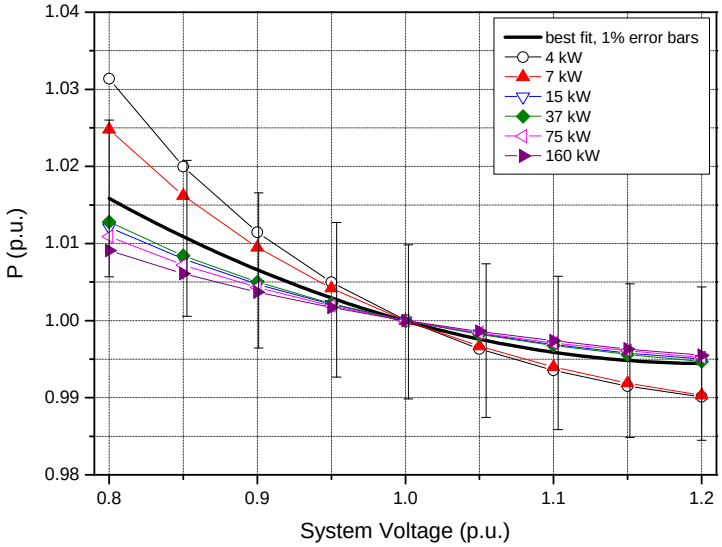


Figure 2.12: *Comparison between active power demand characteristics of directly connected motors of different rated powers.*

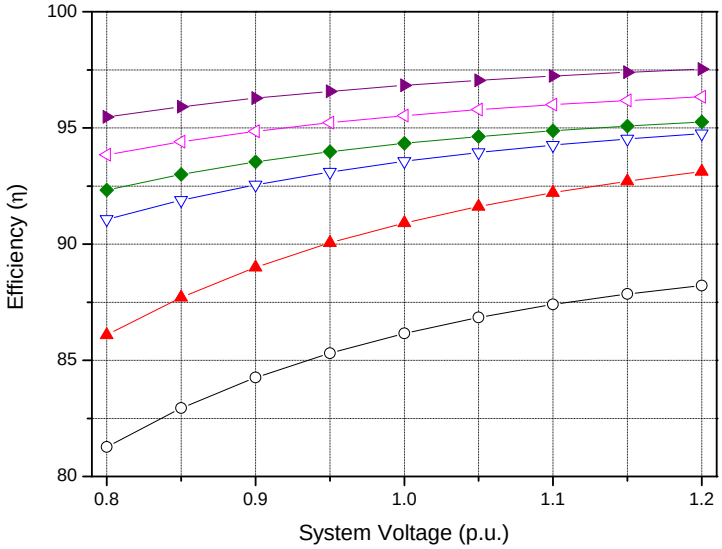


Figure 2.13: *Comparison between efficiencies of directly connected motors of different rated powers.*

2.6.1.2 Reactive power demand and power factor

The changes in reactive power demand with changes in system voltage, Q-V characteristics, are shown for the considered motors in Figure 2.14. It can be seen that motors of different rated powers will have relatively similar Q-V characteristics. The maximum deviation from a line

of best fit (Figure 2.14) is around $\pm 4\%$ in the considered voltage range. But this deviation is reduced to less than $\pm 2\%$ if the voltage range of 0.9-1.1pu is considered.

The change in power factor with system voltage, PF-V characteristics, of the considered motors are shown in Figure 2.15(a). It can be seen that motors of lower rated power will have lower power factors than motors with higher rated power. The PF-V characteristics of the 4kW motor show the largest variation of all considered motors, with the other motors all having similar PF-V characteristics (160 kW motor has lowest variations). In order to compare these characteristics directly, the power factor of each motor can be normalised relative to the nominal motor power factor. The normalised power factors and associated line of best fit of these characteristics for considered motors are shown in Figure 2.15(b). It can be seen that the normalised PF-V characteristics of the considered motors are similar to each other, with a $\pm 3\%$ variation between results over full considered voltage range (0.8 to 1.2pu), and less than $\pm 1.5\%$ variation for the reduced voltage range (0.9 to 1.1pu).

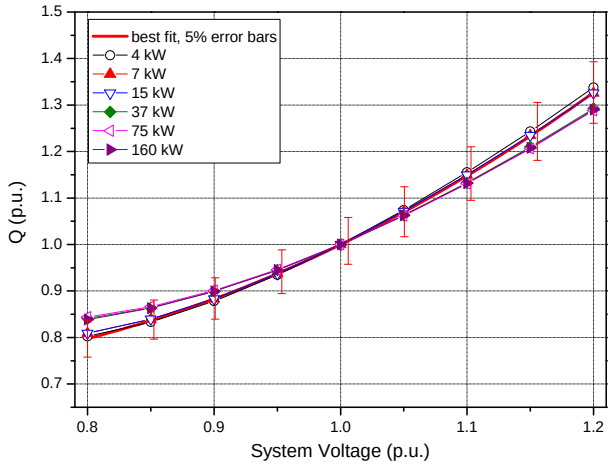
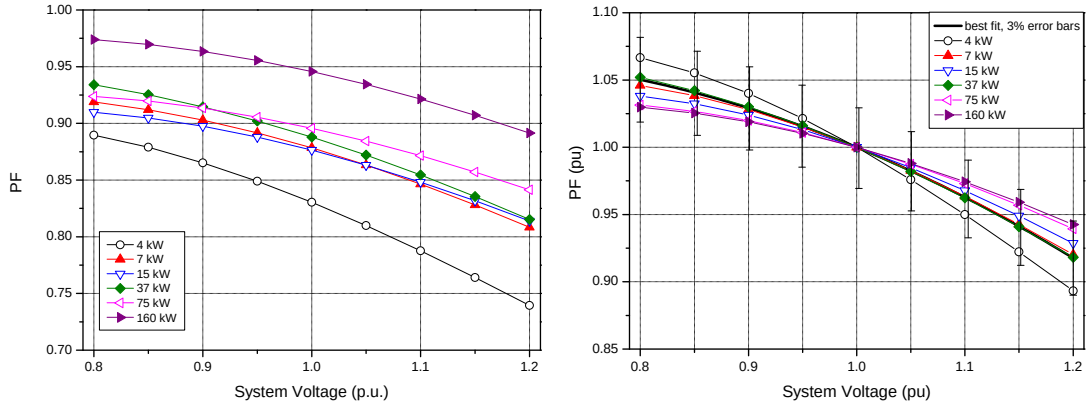


Figure 2.14: *Comparison between reactive power characteristics of directly connected motors of different rated powers.*



(a) Power factor (b) Normalised power factor

Figure 2.15: *Comparison between power factors of directly connected motors of different rated powers.*

2.6.2 Motor loaded with different mechanical loads

The effects of motor mechanical loading on motor P-V and Q-V characteristics are considered next. Two motors are selected for this more detailed investigation: the 4 kW and the 160 kW motors. The 4 kW motor is chosen specifically to represent lower-power motors, as it is in the middle of the power range that makes up over three quarters of the induction motor market (Table 2.1). The 160 kW motor is selected as it represents typical large low voltage motors. The 160 kW motor's P-V and Q-V characteristics also show little variance compared to the other higher power motors (37 and 75 kW). Four general types of mechanical load (as discussed in Section 2.1.1) were applied to each induction motor and simulations were run. Figures 2.16 and 2.17 show these results.

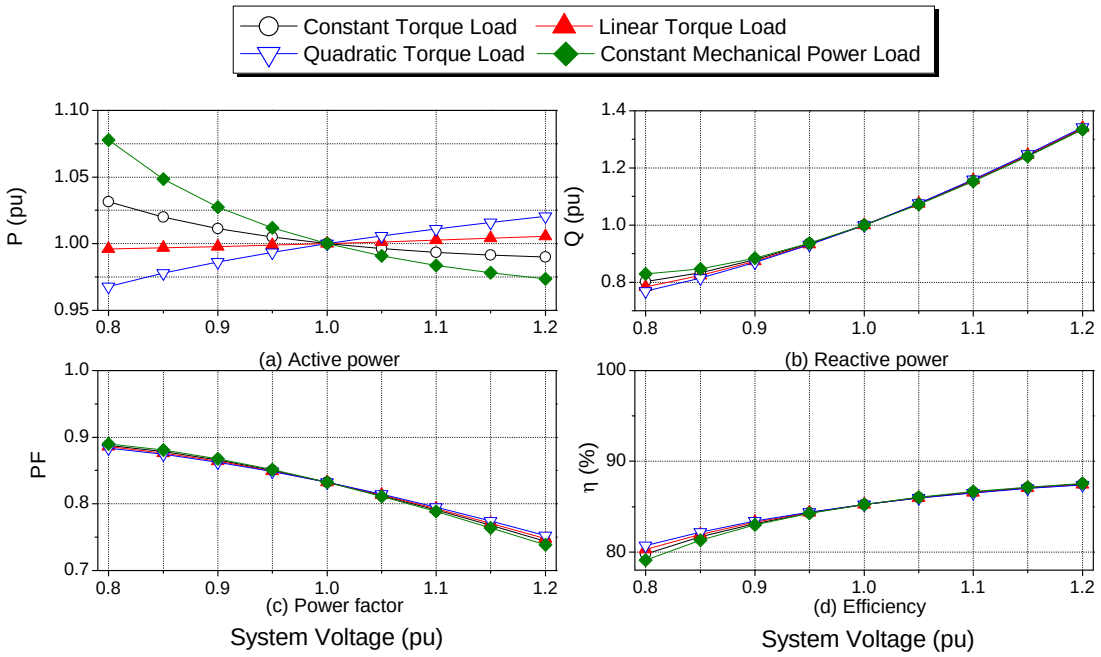


Figure 2.16: *Characteristics of a directly connected 4kW three-phase motor for four different types of mechanical loading.*

It can been seen from Figure 2.16 that the P-V characteristics of the 4 kW motor will be significantly influenced by the mechanical loading applied to the motor. A maximum difference of 11% in P-V characteristics occurs between quadratic and constant mechanical power load at 0.8pu system voltage. This difference reduces as system voltage approaches nominal and then increases again to a value of 4% at 1.2pu system voltage. The motor mechanically loaded with linear torque shows a fairly constant P-V characteristic. For the motor loaded with constant torque or constant mechanical power load, active power consumption is increased with reduction in system voltage. This is because the motor is now supplying similar or the same mechanical power at lower values of system voltage as at 1pu, but this time at reduced motor efficiency, Figure 2.16(d). Quadratic torque motor loading has the opposite effect on the

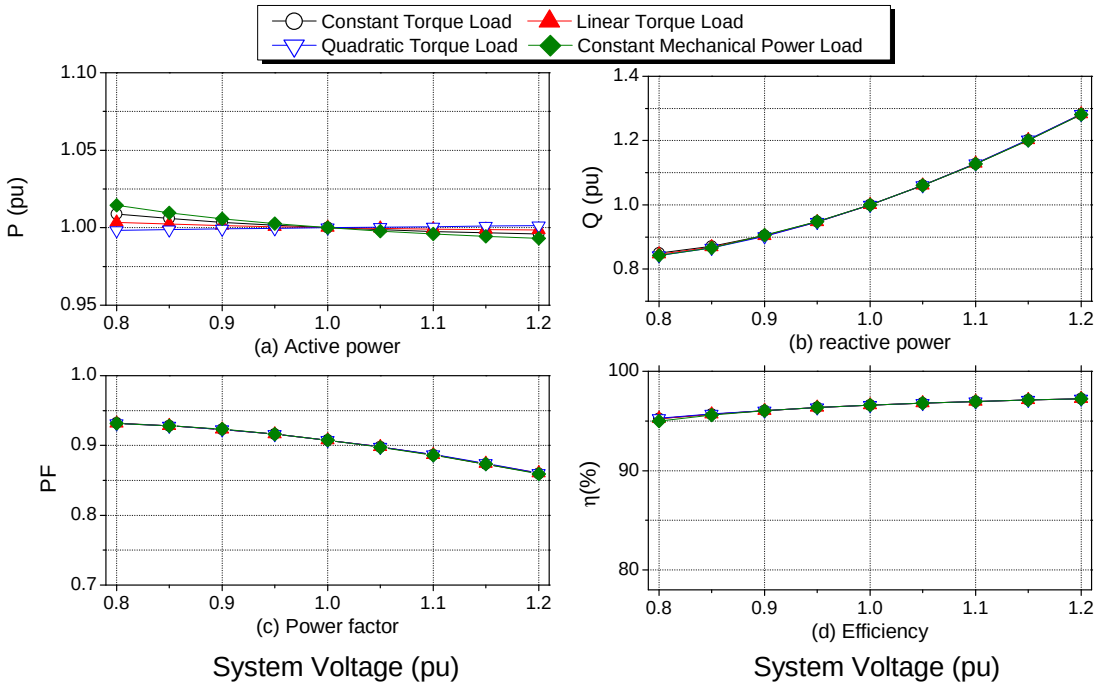


Figure 2.17: *Characteristics of a directly connected 160kW three-phase motor for four different types of mechanical loading.*

4kW motor's P-V characteristics, with active power consumption reducing with reduction in system voltage. This is because the quadratic relationship between torque and speed leads to a fairly significant reduction in required torque at lower motor speeds (i.e. due to lower system voltage) compared to the other considered mechanical loads, see Figure 2.1.

The PF-V, Q-V and $\eta - V$ characteristics of the 4kW motor, on the other hand, will vary little with the change of mechanical loading condition. These characteristics are influenced mainly by the changes in the supply system voltage. This is because the magnetising current (i.e. reactive element of motor current) drawn by the motor will predominantly be a function of system voltage. The reason for this can be explained from observing the motor equivalent circuit in Figure 2.7, where the motor magnetisation branch is electrically parallel to the supply system voltage.

Figure 2.17 shows that the variations in P-V characteristics of the 160 kW motor when motor loading is changed are far less pronounced than for 4 kW motor. This is because the efficiency of the 160 kW motor shows only a small variation, 3%, over the considered voltage range, compared with 9% variation for the 4 kW motor. Thus, the maximum difference in active power demand between different mechanical loading types is less than 1.5%, for the considered range of system voltage (0.8 to 1.2pu). It can also be seen from the results presented in Figure 2.17 that the PF-V, Q-V and $\eta - V$ characteristics of the 160 kW motor are essentially independent of the type of motor mechanical loading.

2.7 Exponential and polynomial load models of three-phase directly connected motors

Exponential and polynomial models of higher and lower power motors are derived from the result presented in Section 2.6. The least square curve fitting method is used to find the coefficients of the exponential and polynomial models. This method is described in the following section.

2.7.1 Least square curve fitting

A standard approach to fit a particular model to a desired data set is to use the least square method. This method achieves the 'best-fit' of a model to observed data when the squares of the model residuals are lowest/least. A model residual is the difference between observed data value and value predicted by the model. In order to explain this method more clearly, an example is now presented.

2.7.1.1 Example of least square method

The P-V characteristics of an example load are given as (0.8,1.073), (0.9,1.016), (1.0,1), (1.1,1.006) and (1.2, 1.022). In order to find the exponential model of this example load, the value of exponential model coefficient np that best represent the example data must be found. According to the least square method, these values of exponential model coefficient np are the values that will give the lowest sum of the squares of model residuals. This problem may also be expressed as shown in (2.8), where the 'best' value of np must be selected to solve presented system of equations.

$$\begin{bmatrix} (0.8)^{np} & = & 1.073 \\ (0.9)^{np} & = & 1.016 \\ (1.0)^{np} & = & 1.000 \\ (1.1)^{np} & = & 1.006 \\ (1.2)^{np} & = & 1.022 \end{bmatrix} \tag{2.8}$$

In order to obtain the 'best' value of np, the minimum value of the function shown in (2.9) must be determined. This can readily be achieved by finding the partial derivative of this function, with respect to np, and setting it zero. This same method may also be used to find the coefficients of the polynomial model, but in this case there will be three unknown parameters, and the solution to the partial differential equations will be more complex. There are various available software tools that directly implement the least square method of curve

fitting, creating and solving the partial differential equations. In this thesis, the MatLab function 'lsqcurvefit' [64] was used.

$$S(np) = [1.073 - (0.8)^{np}]^2 + [1.016 - (0.9)^{np}]^2 + [1.000 - (1.0)^{np}]^2 + \quad (2.9)$$
$$+[1.006 - (1.1)^{np}]^2 + [1.022 - (1.2)^{np}]^2$$

Exponential and polynomial models derived from the example P-V data are shown in Figure 2.18. It can be seen that the exponential model is unable to provide close matching to the example data, because it has only one adjustable parameter, np. Conversely, polynomial model shows much better matching. Therefore, when representing loads with non-linear P-V and Q-V characteristics, the polynomial model will provide better matching than the exponential model.

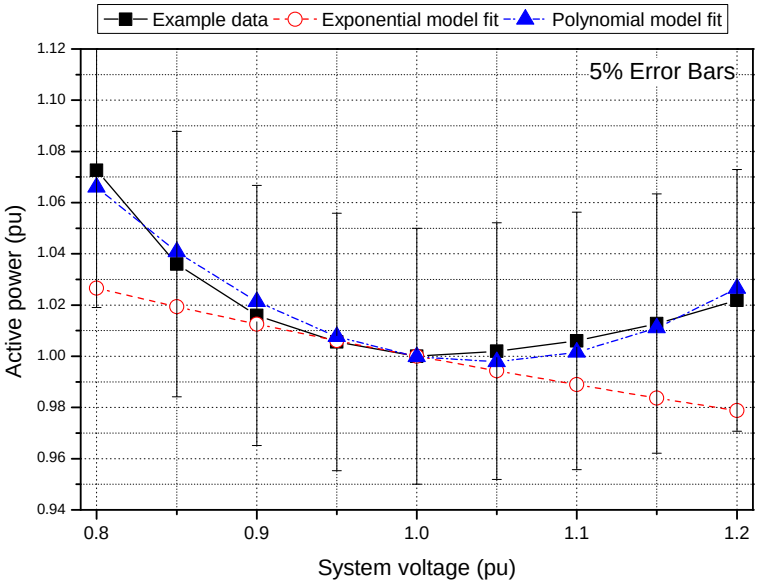


Figure 2.18: *Example data fitting of exponential and polynomial models using the least square method.*

2.7.2 Higher power motors

The previous section has shown that there is only a small variation in the P-V characteristics of the 160 kW motor when different mechanical loads are applied. Furthermore, it has been shown that the P-V characteristics of the 160 kW motor are representative of higher-power motors, i.e. motors with rated active power 15-160 kW. Therefore, the P-V characteristics of the 160 kW motor mechanically loaded with linear torque can be used to represent P-V characteristics of higher-power motor loads without any significant error. The same generalisation can be made

for the Q-V characteristics of higher-power motors, as the Q-V characteristics of the 160 kW motor show even less variation with type of mechanical loading than P-V characteristics. As well, the per-unit Q-V characteristics of the considered higher-power motors are all similar.

The P-V and Q-V characteristics of the 160 kW motor mechanically loaded with linear torque are used to derive exponential and polynomial models of higher-power motor load, using the least square method as presented in Section 2.7.1. The derived exponential and polynomial coefficients are shown in Table 2.6. Figure 2.19 shows plots of these models compared with the original motor data. It can be seen that the polynomial model is able to predict both P-V and Q-V characteristics with only a slight error. However, the exponential model can not exactly match the P-V and Q-V characteristics of the 160 kW motor. Small error is seen in P-V characteristic prediction, but up to 8% error is seen in the prediction of Q-V characteristics.

Table 2.6: *Exponential and polynomial model coefficients of higher power motors.*

Loading	PF_{nom}	Exp. Model		Polynomial Model					
		np	nq	Z_p	I_p	P_p	Z_q	I_q	P_q
All	0.9	-0.01	1.13	0.03	-0.06	1.04	1.60	-2.10	1.5

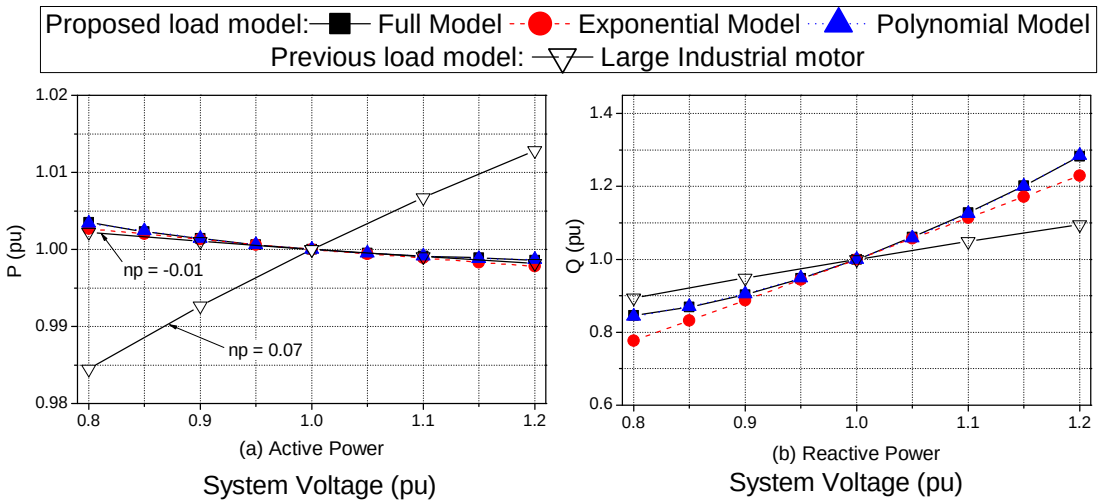


Figure 2.19: *Proposed exponential and polynomial model results for higher power directly connected three-phase induction motors, compared with previous models from existing literature.*

Also shown in Figure 2.19 are existing exponential load models for large industrial motors as presented in Table 2.3. It can be seen that the existing exponential load models suggest a wide possible range of P-V characteristics (np from -0.01 to 0.07), with the proposed models fitting within this range. There was no further information provided in references as to what type of motor mechanical loading was considered in these previous models, or what the definition of 'large' industrial motors is in terms of motor rated power. There were no polynomial models of higher power motors found in literature, so no further comparison with these models can be

made. The comparisons in Figure 2.19 also show that the matching of Q-V characteristics between the previous large industrial motors models and developed motor models are not ideal, although the characteristics are somewhat similar. Again, it is hard to make further comment about the reasons for this mismatching, as there is no further data about the previously developed motor load models. It should be noted that the nominal power factors of proposed and previous models are very similar.

The results presented so far in this chapter with regards to modelling of higher-power directly connected three-phase motors are generally in good agreement with the previous work in this area. But the presented results have additionally shown that the type of motor mechanical loading will have no significant effect on the P-V or Q-V characteristics of higher-power directly connected three-phase induction motors.

2.7.3 Lower power motors

As it has been shown that all considered lower-power motors (4-15 kW) will have very similar P-V and Q-V characteristics, they are represented by the 4 kW motor.

It can be seen from Figure 2.16 that the P-V characteristics of lower-power motors will vary fairly significantly based on the applied motor mechanical loading conditions. Thus, if the approach used in the previous section is adopted, and if all P-V characteristics are assumed to follow a linear torque characteristics, maximum errors of 8%, 3% and 4% in the prediction of motor P-V characteristics, for motors mechanically loaded with constant torque, quadratic torque and constant mechanical power, respectively, would be incurred. The Q-V characteristics of lower-power motors, on the other hand, are essentially independent of type of motor mechanical loading.

Accordingly, when representing the P-V characteristics of lower-power three-phase induction motors, the type of mechanical load the motor is driving should be considered. Table 2.7 presents exponential and polynomial model coefficients of lower-power directly connected three-phase motors, depending on motor mechanical loading condition. Figures 2.20 and 2.21 show these exponential models plotted against the original motor data. Once again, it can be seen that the polynomial model is able to provide more accurate representation of the desired characteristics than the exponential model.

Figures 2.20 and 2.21 also show previously presented exponential models of lower-power industrial motors, Table 2.3. It can be seen that the previous exponential models all have P-V characteristics similar to each other and closely match that of the proposed quadratic torque lower power motor model. There is greater variation/error between the Q-V characteristics of the previous load models of small industrial and air conditioner motor loads with the proposed

load models, and very good match of the previous exponential model of pump/fan load. The power factors of previous load models are higher than those of the proposed load models. It should again be noted that the actual rated power of the previous load models is not known, which may account for the differences in power factors. This can be seen from Figure 2.15 which shows that a 15 kW motor has a similar power factor to those of the previously presented lower power motor models.

It has been shown that the developed models for lower power motors are generally in agreement with the previous work. It has also been shown that when representing the P-V characteristics of lower-power directly connected three-phase motors the type of motor mechanical loading will effect these characteristics and should be considered. However, the Q-V characteristics of these motors are not significantly affected by the type of motor mechanical loading.

Table 2.7: *Exponential and polynomial model coefficients of lower power motors.*

Loading	PF_{nom}	Exp. Model		Polynomial Model					
		np	nq	Z_p	I_p	P_p	Z_q	I_q	P_q
CT	0.83	-0.1	1.44	0.27	-0.63	1.36	1.55	-1.7	1.15
LT	0.83	0.02	1.44	0.02	-0.02	1.0	1.55	-1.7	1.15
QT	0.83	0.13	1.44	-0.15	0.43	0.72	1.55	-1.7	1.15
CP	0.83	-0.25	1.44	0.64	-1.53	1.89	1.55	-1.7	1.15
Where: CT, LT and QT are constant, linear and quadratic torque loads, while CP is constant mechanical power load.									

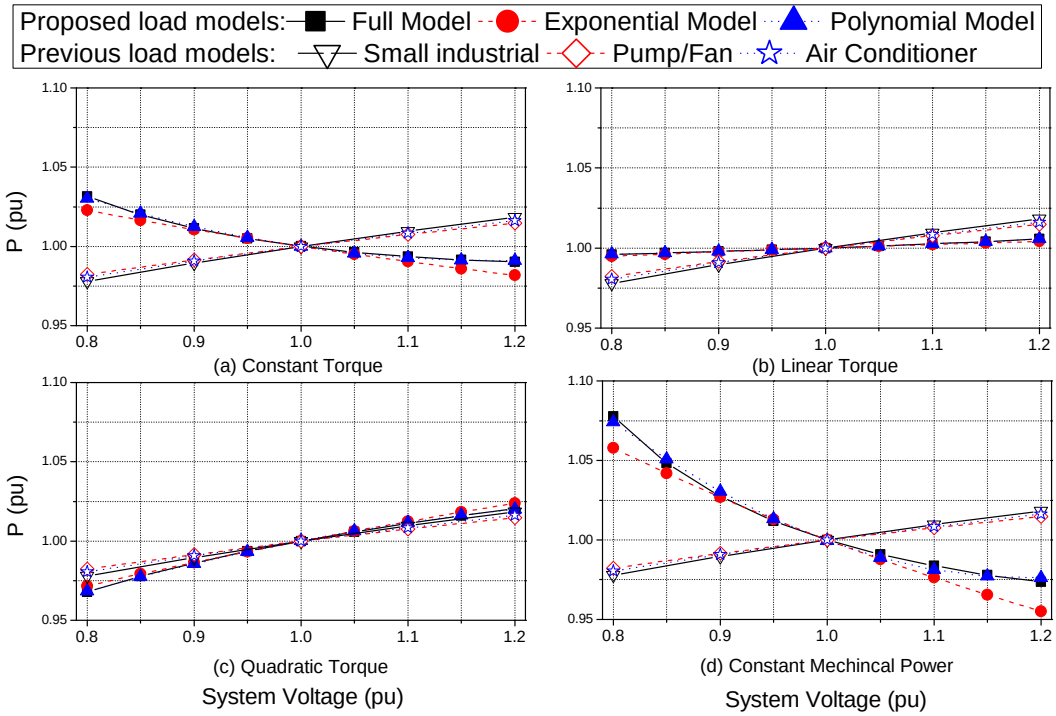


Figure 2.20: *Proposed exponential and polynomial model results for lower power directly connected three-phase induction motors, compared with previous models, P-V characteristics.*

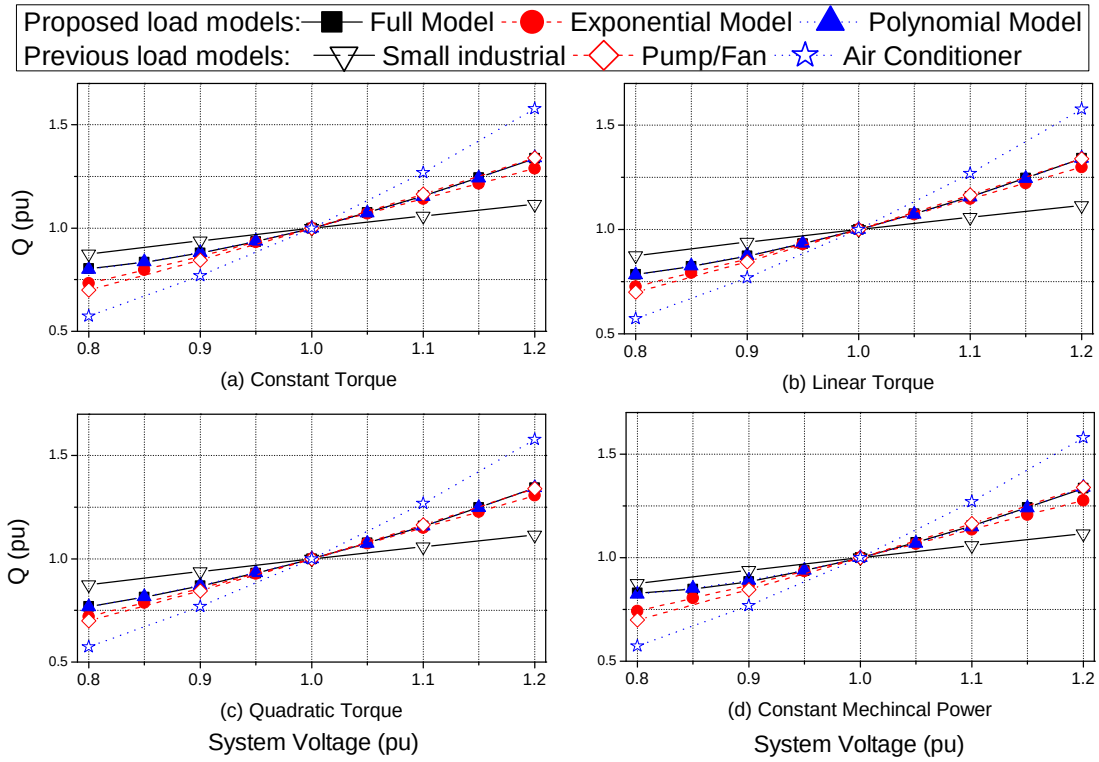


Figure 2.21: *Proposed exponential and polynomial model results for lower power directly connected three-phase induction motors, compared with previous models, Q-V characteristics.*

2.8 Active and non-active power demand characteristics of ASDs

As discussed in the introduction to this chapter, at present there is little specific guidance on the representation of ASDs in power system studies. Thus, investigation into the general characteristics of several typical ASDs of different rated powers, types of drive control and mechanical loading is performed in this section.

2.8.1 Per-unit comparison of ASDs at different rated powers

Similarly to the directly connected motors, the majority of ASDs will be connected to the low voltage system. They will be of rated active power in the range 1 kW to 200 kW. Therefore, the same 4 kW, 15 kW, 75 kW and 160 kW directly connected motors, discussed before, are used to develop ASD models of the corresponding electrical powers. This is achieved by adding standard VSI drives, introduced in Section 2.2, to these motors. Four different drive control strategies were implemented, each representing a different type of ASD. The considered ASD control strategies are: open-loop V/Hz, closed-loop V/Hz, field oriented (FOC) and direct torque control (DTC). As discussed previously, the V/Hz controlled ASD is currently the most common type of ASD. However, it is expected that the number of more advanced types of ASDs (FOC and DTC) will increase over the next years. Hence, they are included in this analysis.

Initially, in order to perform direct comparisons between the ASDs, nominal values of L_{dc} and C_{dc}, as described in Section 2.4, were used. In order to compare ASDs of different rated powers directly, it is important that the applied ASD parameters (L_{dc} and C_{dc}) are in per unit, i.e. scaled to the rated power of the ASD. However, this presents a slight problem when considering system impedance, as although not an ASD parameter, it will have an effect on ASD non-active power demand characteristics (this effect is discussed in more details in Section 2.8.3). For the purposes of this thesis, the typical residential system impedance, as discussed in Section 1.8, is taken as nominal system impedance for the 4 kW ASD. Using this point as reference, the system impedance is converted to a per-unit value and applied to the ASDs of different rated powers. The alternative to this approach is to simply set system impedance to zero for all considered ASDs. However, this is a very unrealistic situation, and will have adverse effects on (modelling) ASD operation, as is discussed in Section 2.8.3.

The characteristics of ASDs of different rated powers and types are now investigated, and the results are presented in Figures 2.22 to 2.25. All considered ASDs were set to run at nominal speed and loaded with constant torque mechanical load. In order to present the results in a concise and compact manner, the non-active power characteristics of the ASDs are represented by the fundamental reactive power (Q_1) and the total harmonic distortion (THD) of the drive input current (for definitions see Section 1.7). The results for both active and fundamental reactive power demand are presented in per unit, enabling direct comparison between ASDs of different rated powers. The per-unit bases are taken as the active and fundamental reactive power demand of the considered ASD when operated with nominal values of dc link filter components, nominal system impedance, mechanically loaded with nominal load, run at nominal speed and supplied by nominal system voltage. The efficiency (η) of the ASDs is expressed as a percentage, and defined as the ratio of the output (motor) mechanical power to input (drive) electrical power.

2.8.1.1 V/Hz open-loop controlled ASDs

The P-V characteristics of the open-loop V/Hz operated ASDs are presented in Figure 2.22(a). They have a similar shape to those of the directly connected motors, previously discussed in Section 2.6.1.1. Due to drive losses, the open-loop ASDs will, however, draw more active power to supply the same constant torque mechanical load. The effect of drive losses can be seen in Figure 2.22(d), where ASDs are around 3-5% less efficient than directly connected motors (Figure 2.13). At lower values of system voltage (less than 1.0pu), a clear difference can be observed between the P-V characteristics of lower power 4 kW open-loop ASD and higher power 15 kW, 75 kW and 160 kW open-loop ASDs. At higher values of system voltage (greater than 1pu), all considered open-loop ASDs exhibit more similar P-V characteristics. This is due to the $\eta - V$ characteristics of the open-loop ASDs, which all show reduction in efficiency at lower values of system voltage, with the 4 kW ASD showing the greatest reduction. At higher

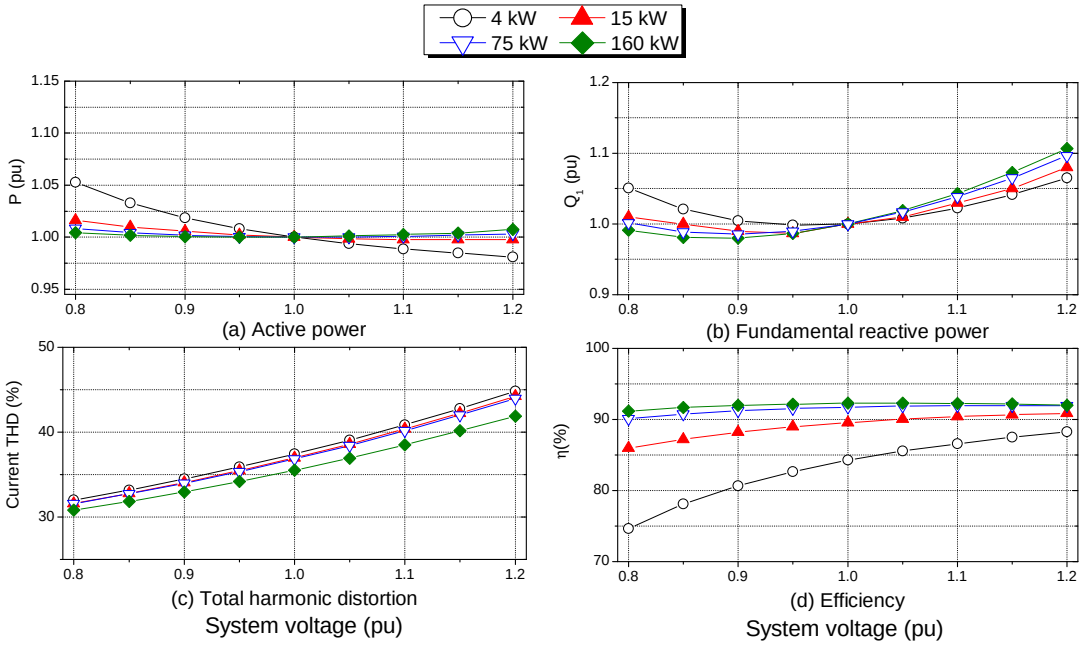


Figure 2.22: *Comparison of 4 kW, 15 kW, 75 kW and 160 kW V/Hz open-loop controlled ASD characteristics, mechanically loaded with constant torque load.*

values of system voltage, the efficiencies of all the open-loop ASDs are much more similar. Non-active power characteristics are discussed in Section 2.8.1.4.

2.8.1.2 V/Hz closed-loop controlled ASDs

The closed-loop V/HZ operated ASD P-V characteristics are shown in Figure 2.23(a). These P-V characteristics show that the ASDs draw more active power at lower values of system voltage, and have similar powers at higher system voltages when compared to open-loop ASDs. This is due to the closed-loop control, acting to keep the ASD speed constant with change in system voltage. As the closed-loop ASDs are loaded with constant torque load, the resulting mechanical power is constant with respect to change in system voltage. Thus, compared to open-loop ASDs, closed-loop ASDs will draw more active power at lower values of system voltage and less active power at higher values of system voltage. The increased consumption of active power at lower values of system voltage also results in slightly increased losses in the closed-loop ASDs, Figure 2.23(d). This will further increase the difference in P-V characteristics between open-loop and closed-loop ASDs. Again, it can be seen that there is a clear distinction between the P-V characteristics of lower-power and higher-power closed-loop ASDs, at lower values of system voltage. Considered closed-loop ASDs all have similar P-V characteristics at higher values of system voltage. Their non-active power characteristics are discussed in Section 2.8.1.4.

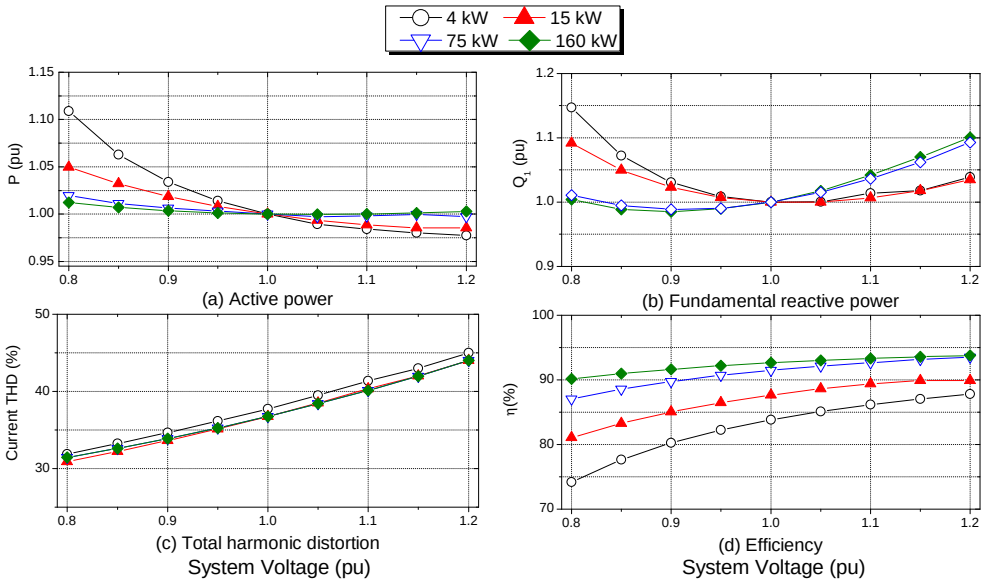


Figure 2.23: *Comparison of 4 kW, 15 kW, 75 kW and 160 kW V/Hz closed-loop controlled ASD characteristics, mechanically loaded with constant torque load.*

2.8.1.3 ASDs with advanced drive control

The P-V characteristics of ASDs with advanced drive controls (FOC and DTC), are shown in Figures 2.24(a) and 2.25(a) respectively. It can be seen that both types of ASDs operate in essentially the same manner from a load modelling viewpoint. The P-V characteristics are essentially constant and very similar for all considered ASD rated powers. This is due to the advanced drive control, regulating the motor speed and keeping the losses constant. Hence, the efficiency of the ASDs is also constant with changes in system voltage.

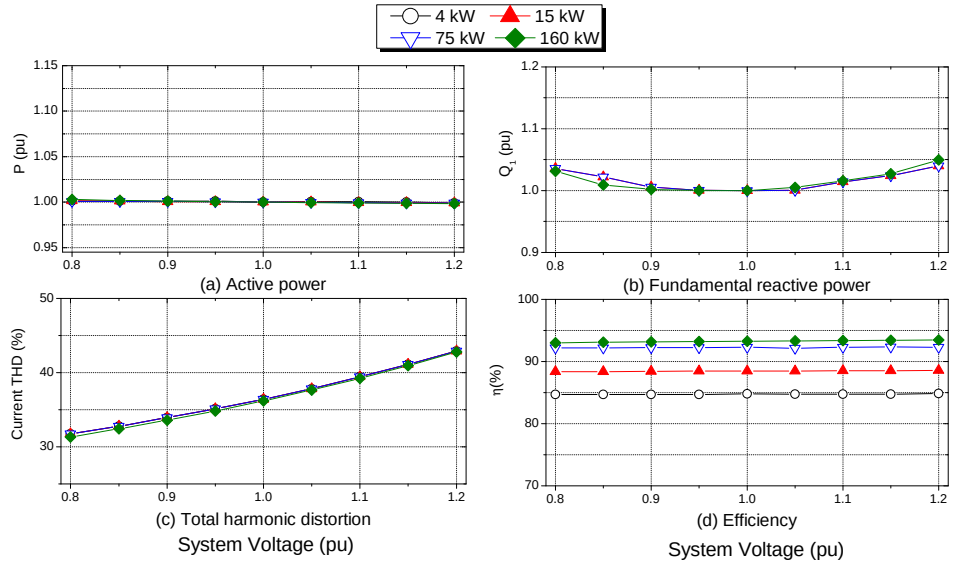


Figure 2.24: *Comparison of 4 kW, 15 kW, 75 kW and 160 kW field oriented control ASD characteristics, mechanically loaded with constant torque load.*

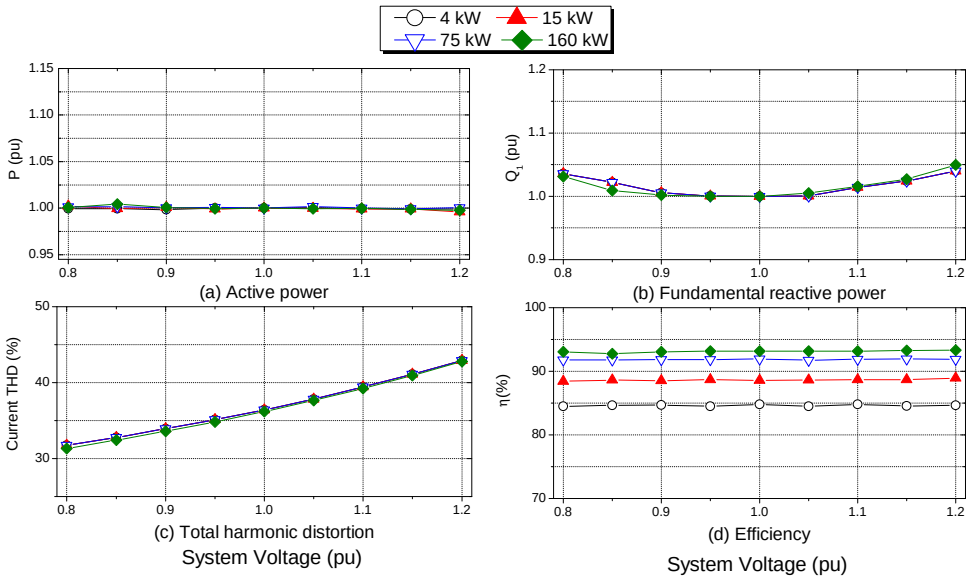


Figure 2.25: *Comparison of 4 kW, 15 kW, 75 kW and 160 kW direct torque controlled ASD characteristics, mechanically loaded with constant torque load.*

2.8.1.4 Non-active power characteristics

Figures 2.22 to 2.25, subplots (b) and (c) show the non-active power demand characteristics of the considered ASDs. From comparison of these results it can be seen that the Q_1-V characteristics of the ASDs are influenced by the P-V characteristics of the ASD. The results in Figures 2.24 and 2.25 help to show that the type of the ASD has no significant effect on ASD non-active power characteristics. This is further confirmed by observing the THD-V characteristics of all considered ASDs, which are very similar to each other. This is because these characteristics are dominated by the front-end bridge rectifier, dc link filter and to a much lesser extent the system impedance, which in this analysis is common (due to per-unit values being selected) to all considered ASDs. These non-active power demand characteristics of ASDs are discussed further in Section 2.8.3.

2.8.2 Characteristics of ASDs with different types of mechanical loading conditions

The effect of motor mechanical loading on ASD P-V and N-V characteristics are considered next. The two ASDs selected for this more detailed investigation are the 4 kW and the 160 kW ASDs, for the same reasons discussed in Section 2.6.2. These ASDs are set up in exactly the same way as in the previous analysis, albeit with the application of different mechanical loads.

2.8.2.1 V/Hz open-loop operated ASDs

The P-V characteristics of the open-loop controlled 4 kW and 160 kW ASDs loaded with the four common types of mechanical load are shown in Figures 2.26(a) and 2.27(a) respectively. From these results it can again be seen that the P-V characteristics of both ASDs are similar to those of the directly connected motors with corresponding powers. The 4kW ASD exhibits a maximum difference of 17% in active power between ASD mechanically loaded with quadratic torque and constant mechanical power loads at 0.8pu system voltage. This is compared to a 2% variation in the 160 kW ASD. The differences are smaller at higher values of system voltage, but are still around 10% for the 4 kW ASD and less than 1% for the 160 kW ASD. The $\eta - V$ characteristics of both open-loop ASDs (Figures 2.26(d) and 2.27(d)) are similar in shape to the corresponding directly connected motors, although with lower values due to drive losses. Additionally, as the maximum difference between active power consumption is now 17% for the 4 kW ASD (previously 10% for the directly connected motor), it is apparent that the drive losses will not be constant with voltage.

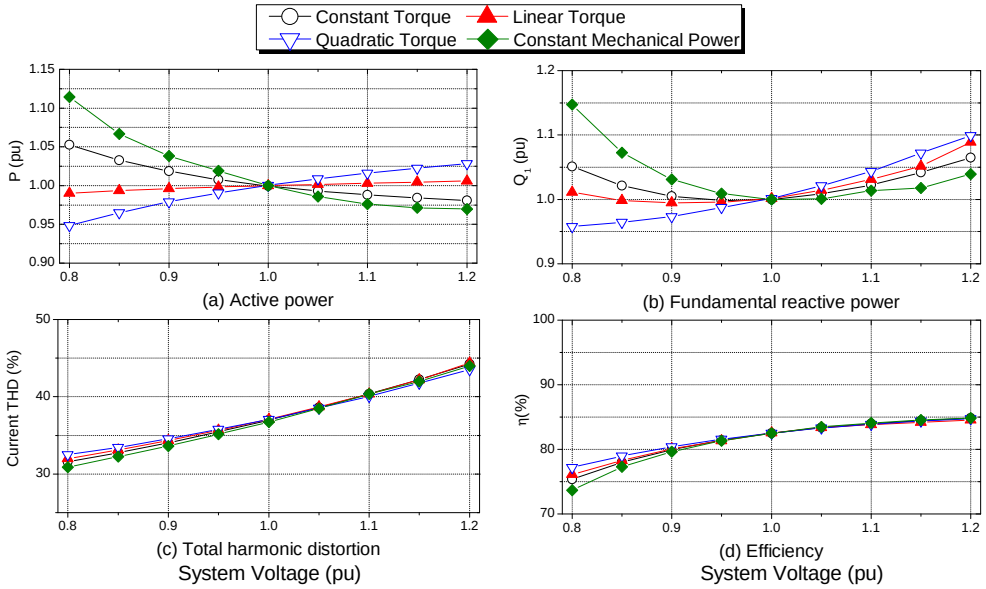


Figure 2.26: *Characteristics of 4 kW open-loop operated ASDs, for four types of mechanical loading.*

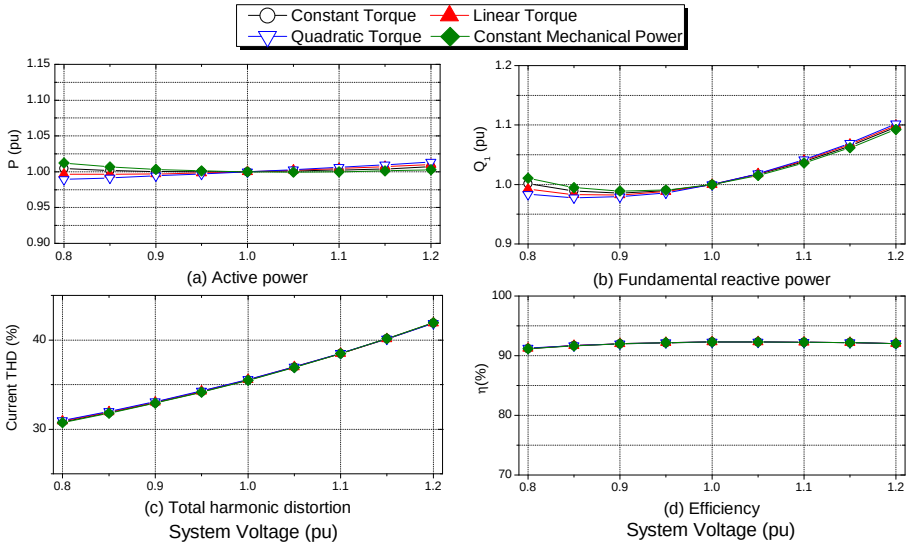


Figure 2.27: *Characteristics of 160 kW open-loop operated ASDs, for four types of mechanical loading.*

2.8.2.2 V/Hz closed loop operated ASDs

Figures 2.28 and 2.29 show the results of the analysis for closed-loop operated 4 kW and 160 kW ASDs. It can be seen that for all considered mechanical loading conditions, P-V and $\eta - V$ characteristics correspond to that of the open-loop operated ASD loaded with a constant power mechanical load (as explained in Section 2.8.1.2). This is because the drive will control the speed of the motor so that it is constant with the changes in supply system voltage magnitude, keeping the mechanical power drawn from the motor constant. The slight variation in the results is due to the allowed $\pm$ 1% error band in adjusted speed of the implemented closed-loop ASD controller.

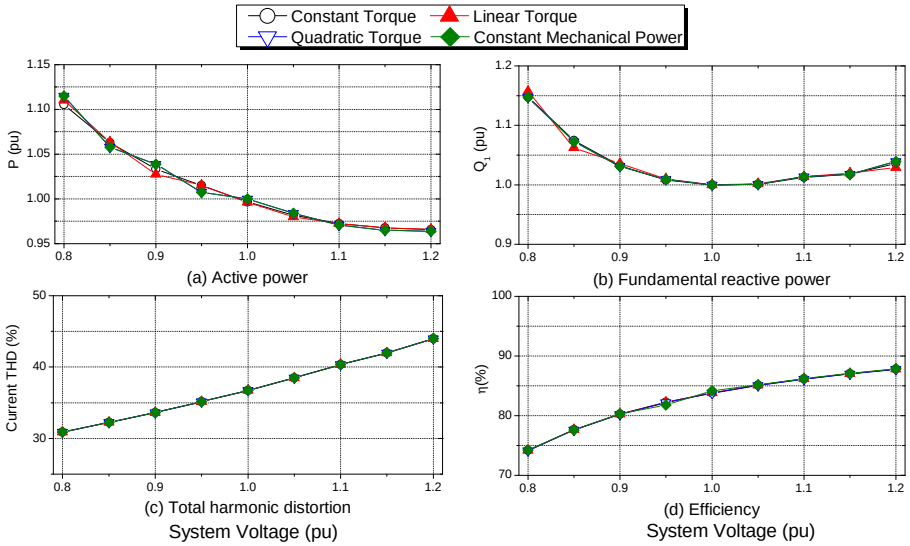


Figure 2.28: *Characteristics of 4 kW closed-loop operated ASDs, for four types of mechanical loading.*

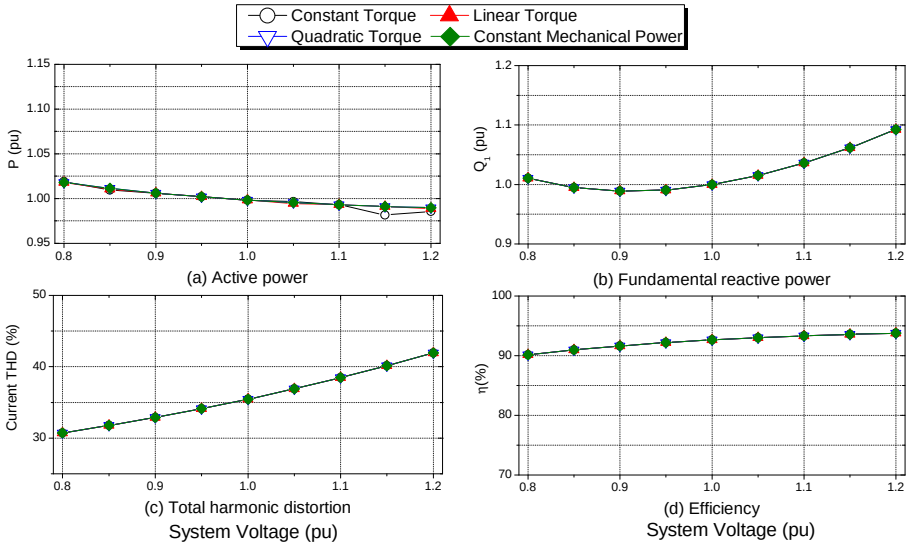


Figure 2.29: *Characteristics of 160 kW closed-loop operated ASDs, for four types of mechanical loading.*

2.8.2.3 Advanced drive controlled

The comparisons of the advanced drive controls are presented in Figures 2.30 to 2.33, illustrating that their P-V characteristics are independent of the type of motor mechanical load. All ASDs show constant P-V characteristics for the considered voltage range. Both types of advanced drive controls have essentially the same characteristics for all considered power quantities. Again, this is due to the method of drive control that keeps motor speed and therefore mechanical loading constant, maintaining constant losses.

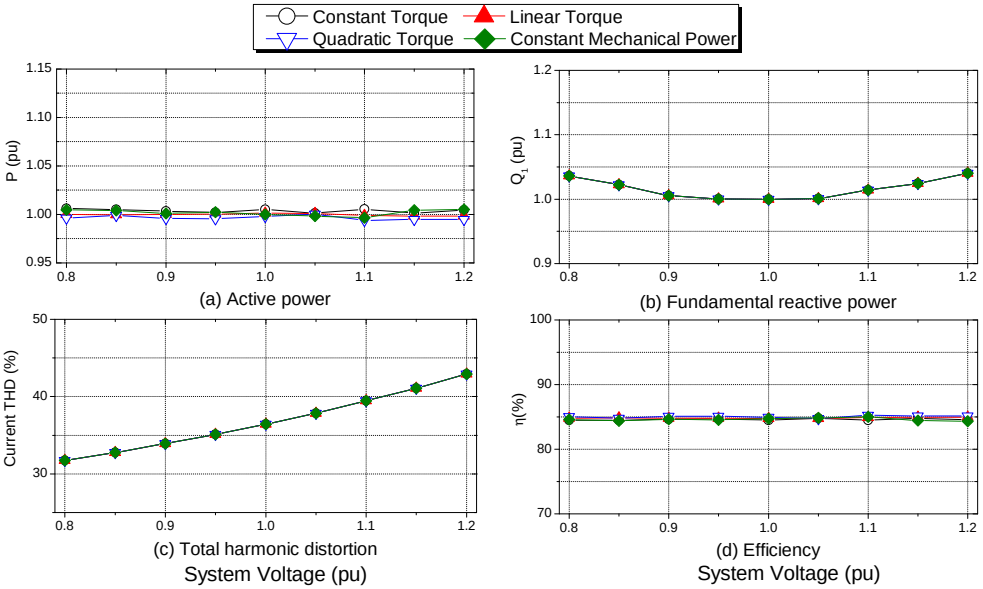


Figure 2.30: *Characteristics of 4 kW direct torque controlled ASDs, with four types of mechanical loading.*

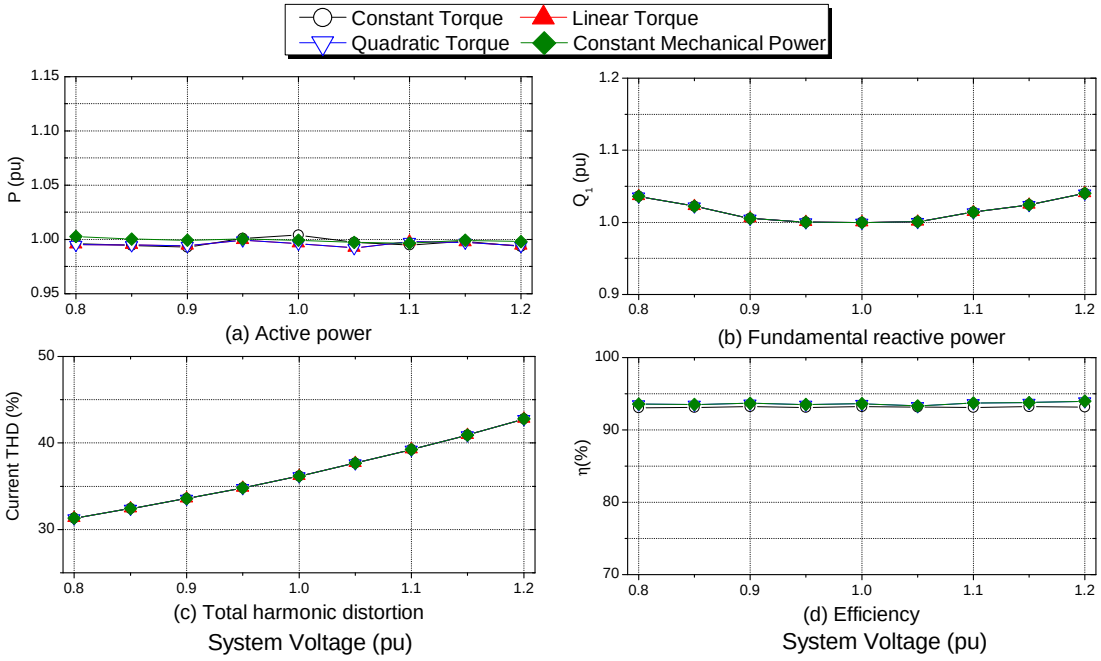


Figure 2.31: *Characteristics of 160 kW direct torque controlled ASDs, with four types of mechanical loading.*

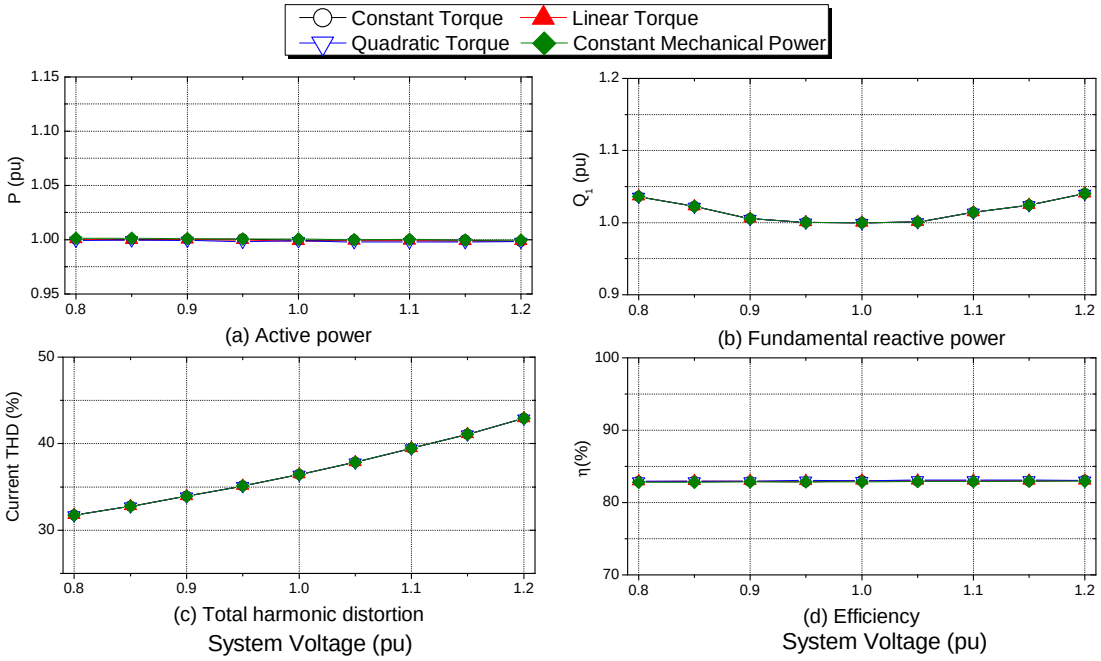


Figure 2.32: *Characteristics of 4 kW field oriented controlled ASDs, with four types of mechanical loading.*

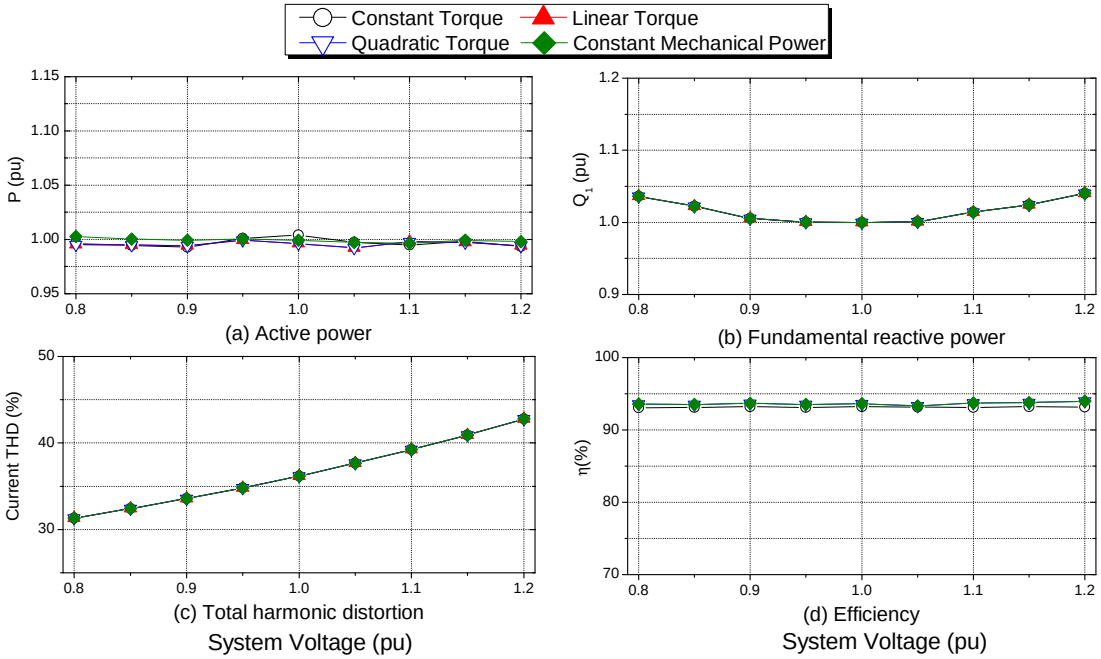


Figure 2.33: *Characteristics of 160 kW field oriented controlled ASDs, with four types of mechanical loading.*

2.8.2.4 Non-active power demand characteristics

The results of the comparison between the non-active power demand characteristics of the considered ASDs for different mechanical loads are shown in Figures 2.26 to 2.33, subplots (b) and (c). It can again be seen that ASD non-active power characteristics are influenced by ASD active power characteristics. The shape and magnitude of these non-active power characteristics and how they depend on system impedance, ASD dc link filter components, ASD active power demand and change in system voltage are all discussed in the following section.

2.8.3 Effect of dc link filter components and system impedance on characteristics of ASD

Detailed discussion of ASD non-active power demand characteristics has been postponed until this section, as these characteristics depend mainly on the value of dc link filter components, and to a lesser extent, system impedance. As shown in the previous subsections, the type and rated power of the ASD will have little effect on non-active power characteristics. Therefore, the 4 kw open-loop controlled ASD is used for this analysis and is taken as being representative of all considered ASDs.

Firstly, the effect of system impedance on the characteristics of the 4 kW ASD are considered. Figure 2.34 shows the P-V and N-V characteristics of the 4 kW ASD for applied minimum,

nominal and maximum values of system impedance. The, minimum and maximum typical values of system impedance are taken as being $\pm$ 50% of the nominal value of system impedance, as defined in Section 1.8. Next, the effect on ASD characteristics of altering the dc link components, i.e. C_{dc} and L_{dc} is investigated. The information presented in Section 2.4 is used to define maximum, nominal and minimum values of C_{dc} and L_{dc}, with minimum value of L_{dc} taken as zero. Figure 2.35 shows the results of this analysis with system impedance taken as nominal.

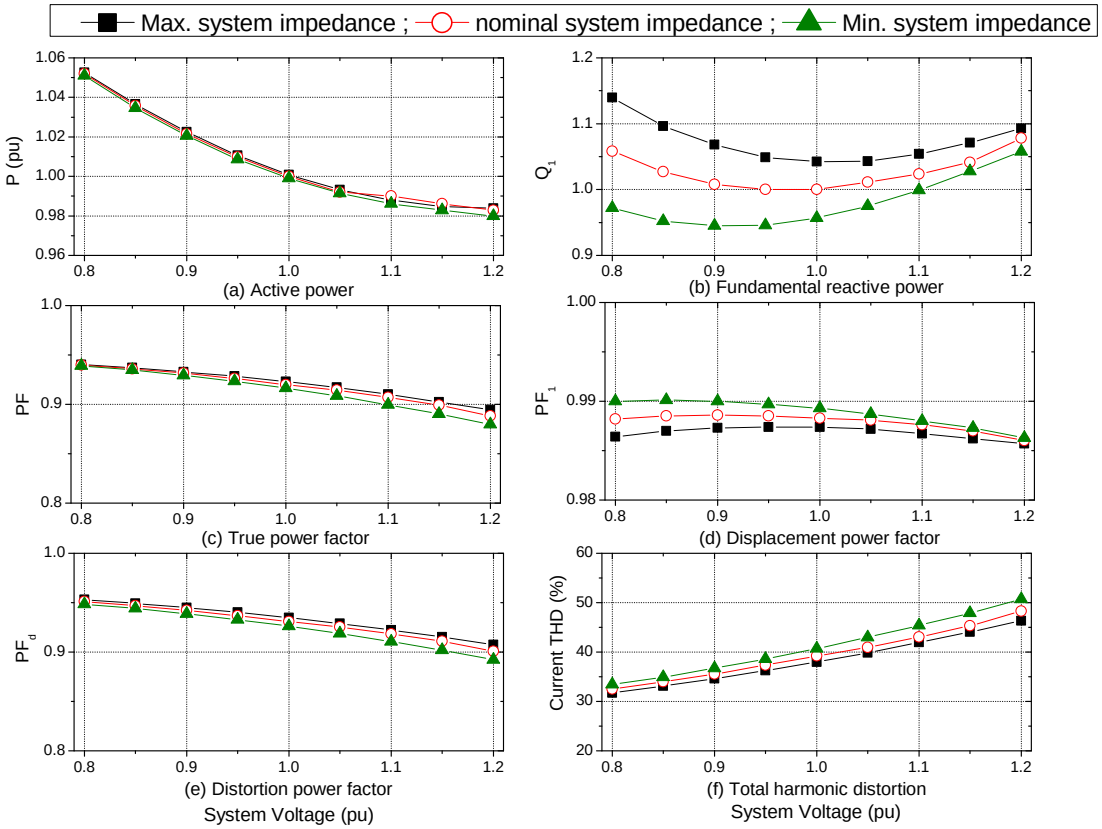


Figure 2.34: *Comparison between 4 kW open-loop V/Hz controlled ASD for maximum, nominal and minimum values of system impedance and motor loaded with constant torque load.*

2.8.3.1 Discussion of characteristics

The results presented Figure 2.34 show that change in value of system impedance will have essentially no effect on the P-V and a slight effect on the N-V characteristics of the ASD. Two reasons why the system impedance affects the N-V characteristics of the ASD are: a) it will dictate the rate of rise and rate of fall of the ASD input current during the ASD commutation subinterval (assuming ASD is operating in continuous current conduction mode) and b) it will have an effect on the shape of the ASD input current waveform during the conduction subinterval (for full discussion see Section 2.11). Therefore, change in system impedance

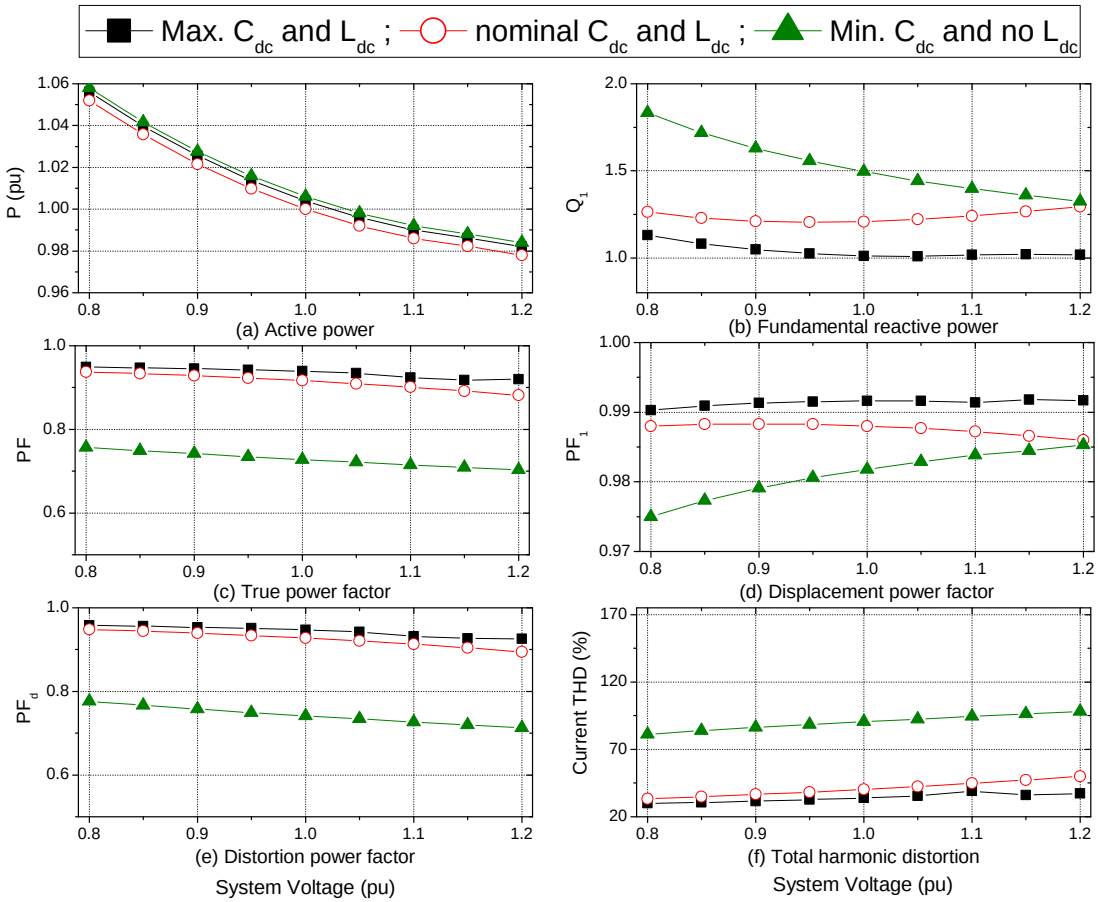


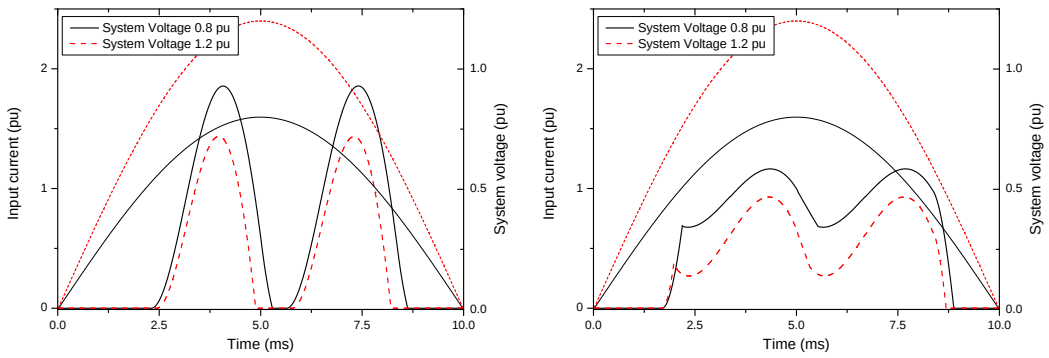
Figure 2.35: *Comparison between 4 kW open-loop V/Hz controlled ASD for a range of dc link components values, nominal system impedance and motor loaded with constant torque load.*

will affect the shape of the ASD input current waveform and hence alter the non-active power characteristics of the ASD. It can be seen that the difference in Q_1-V characteristics between minimum and maximum values of system impedance is greatest at 0.8pu system voltage, with a difference of 10% in the prediction of fundamental reactive power demand. However, it should be noted that the displacement power factor of the ASD at nominal voltage only changes from 0.987 to 0.989 between minimum and maximum values of system impedance. As PF_1 is close to unity, this small change has a relatively large effect on per-unit Q_1-V characteristics, although the effect on absolute reactive power flow will not be significant (as Q_1 is low). The difference between the current THD of the ASD at maximum and minimum values of system impedance is approximately 6.5% at nominal voltage, increasing to a maximum value of approximately 10% at 1.2pu system voltage. Thus, the value of the system impedance will have little influence on the harmonic content of the ASD current waveform.

The effect of changing the values of dc link filter components on ASD power characteristics is shown in Figure 2.35. It can be seen that ASD P-V characteristics are essentially independent

of the values of dc link filter components for the considered range of values. However, Figure 2.35(d) shows that larger values of dc link filter components result in higher ASD displacement power factors. Accordingly, the ASD will consume less reactive power for higher C_{dc}/L_{dc}. Also, the gradient of the Q_1-V characteristics will change depending on the dc link filter components (negative for minimum values and positive for nominal and maximum values). This occurs because the value of L_{dc} dictates the mode of ASD operation, which can be either continuous or discontinuous (as explained in Section 2.2.1.2). Low or zero values of L_{dc} result in the ASD operating in discontinuous current conduction mode. In this mode of operation, the ASD input current consists of two distinct pulses, Figure 2.36(a). As system voltage is increased, these pulses narrow and the peaks reduce in magnitude, making the pulses slightly more symmetrical with respect to the system voltage maximum and therefore the displacement power factor increases. Conversely, when the ASD operates in continuous current conduction mode, the two distinct input current pulses per half-cycle merge to a single current pulse, Figure 2.36(b). In this situation, as the input current pulse is continuous, narrowing of the pulse at higher values of system voltage leads to a reduction in the displacement power factor, as the current waveform is less symmetrical.

Further, Figure 2.35 shows that higher values of dc link filter components lead to less distortion in the ASD input current, (the same effect can be seen when system impedance is increased). This is occurs because any increase in inductance in the ASD conduction path will act to suppress harmonics, as discussed in Section 2.5.



(a) Discontinuous current conduction mode (b) Continuous current conduction mode

Figure 2.36: *Effect on ASD current waveforms with change in system voltage when ASD operates in discontinuous and continuous current conduction modes.*

2.9 Summary of presented ASD characteristics

The P-V characteristics of lower and higher power V/Hz open-loop controlled ASDs have been shown to be very similar to those of the associated directly connected motors. As in the case of directly connected motors, the mechanical loading of the ASD should be taken into account

when considering P-V characteristics of lower power ASDs, while a single characteristics for all mechanical loading types maybe be assumed for higher power V/Hz open-loop controlled ASDs. V/Hz closed-loop controlled ASDs have been shown to have the same P-V characteristics as open-loop V/Hz ASDs mechanically loaded with constant mechanical power. Finally, advanced drive controlled ASDs will have constant P-V characteristics for both lower and higher power ASDs. From analysis in Section 2.8.3, it has also been shown that P-V characteristics of all considered types of ASDs are essentially independent of dc link filter components and value of system impedance.

Non-active power characteristics of ASDs, however, are influenced by ASD P-V characteristics, values of L_{dc} and C_{dc} and slightly by supply system impedance. Standard polynomial and exponential load models can not represent these characteristics, and more detailed load models must be developed. These models are developed and validated in the next section, where further investigation of the characteristics of ASDs is performed.

2.10 Equivalent circuit model of drive-controlled motors

The previous section has shown that non-active power characteristics of drive controlled motors are substantially influenced by the values of C_{dc}, L_{dc} and to a much lesser extent the system impedance. Active power demand characteristics are relatively unaffected. This complicates the analysis of three-phase ASD, compared to that of directly connected three-phase motors, as exponential and polynomial expressions that accurately describe the ASD's non-active power characteristics can not be easily fit for the possible wide range of values of dc link filter components and values of system impedance. Additionally, these models can not represent the harmonic characteristics of ASD loads. Therefore, a new approach for the representation of ASD non-active power demand characteristics must be adopted. In developing the new approach, the open-loop V/Hz controlled 4 kW ASD will be primarily investigated.

2.10.1 Equivalent representation of ASD bridge, inverter and motor

Previous work focussing on the subject of harmonic modelling of ASDs, [57], [58], [60] and [65] has shown that it is possible to replace the motor and inverter in the ASD with an equivalent load, i.e. with an equivalent current source ([58]), or equivalent resistance ([57]), or equivalent constant power load, ([60] and [65]). Accordingly, Figure 2.37 shows such an equivalent model of three-phase ASD. The model includes a resistance to represent the combination of the motor and the inverter. In previous work, as the focus of the analysis has been solely on harmonic studies, this equivalent resistance is commonly set at a fixed value, [57]. This fixed value is usually selected so the equivalent ASD model draws the desired active power at 1pu voltage,

with ASD P-V characteristics assumed constant. However, the previous section has shown that this assumption is only valid for certain types of currently not widely used types of ASDs. The most common types of ASDs, at present, are V/HZ controlled drives, which have non-constant P-V characteristics. Therefore, for the these types of ASDs, the equivalent resistance should vary in such a way as to produce P-V and N-V characteristics that closely match those of the full drive and motor model.

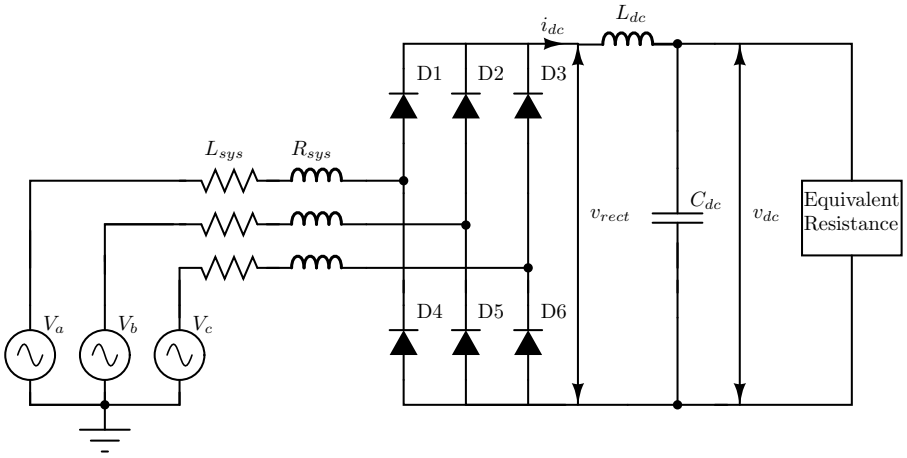


Figure 2.37: *Equivalent circuit model of ASD.*

In order to achieve required matching of ASD active and non-active power demand characteristics, the relationship between the active power drawn from the dc link, P_{dc}, and the rms value of the dc link voltage, V_{dc} was investigated. Figure 2.38(a) shows this comparison for the 4 kW open-loop V/Hz controlled ASD, loaded with the four considered types of mechanical loads. It can be seen that the active power drawn at the dc link follows a very similar characteristic shape for all considered mechanical loading conditions as that of the input active power drawn by the ASD in Figure 2.26. The only difference is that there are no rectifier losses. The results shown in Figure 2.38 are in per unit, where base voltage is the rms input phase voltage and base power is nominal active power of the 4 kW directly connected motor at the dc link.

Equivalent resistance may be calculated using the standard relationship in (2.10).

$$R_{dc} = \frac{V_{dc}^2}{P_{dc}} \tag{2.10}$$

Therefore, the power drawn from the ASD dc link may be represented as an equivalent resistance that is a function of dc link rms voltage, which in turn is a function of supply system voltage and dc link component values. The change in equivalent resistance with dc link rms voltage is shown in Figure 2.38(b), again for the four considered mechanical loading conditions.

From the results in Figure 2.38(b), corresponding analytical expressions can be developed, as

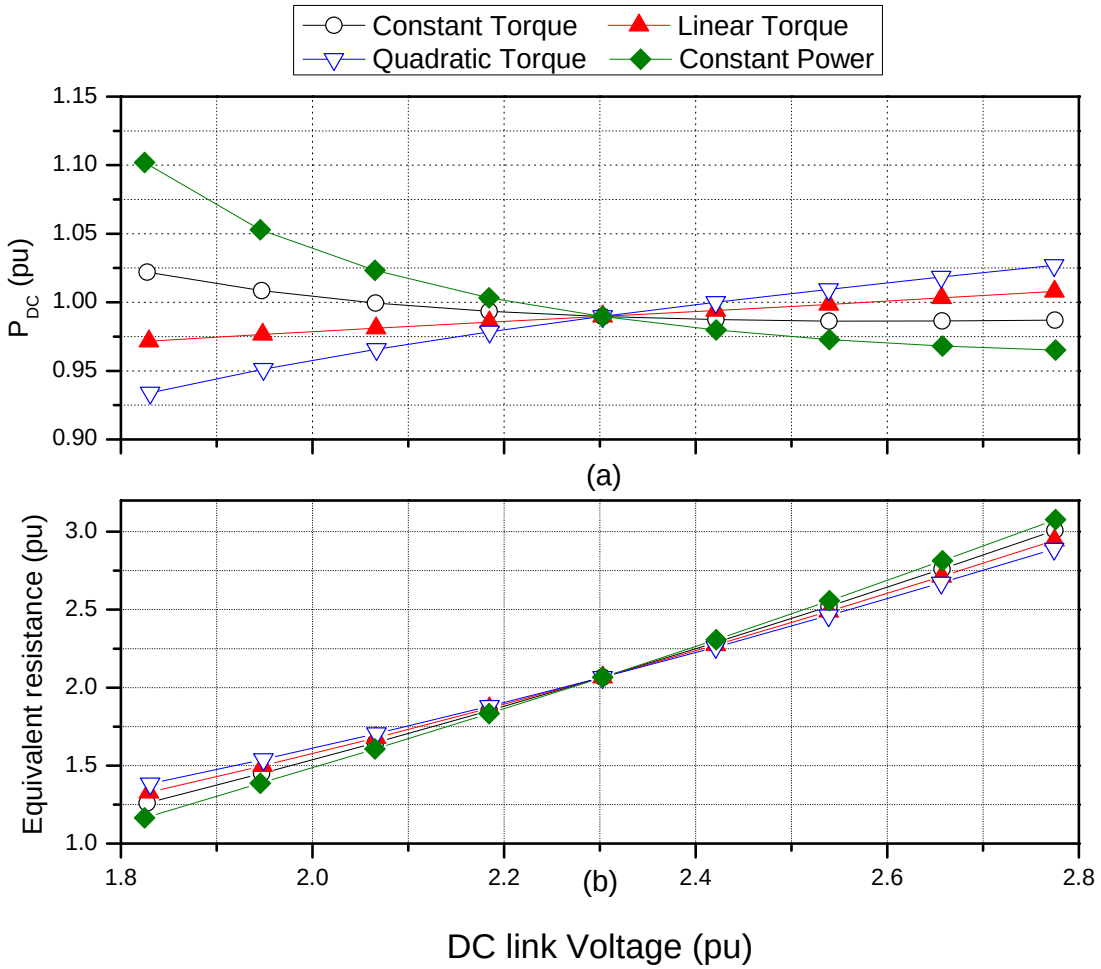


Figure 2.38: *a)Power drawn at ASD dc link, b) Equivalent resistance versus the rms dc link voltage for the four considered types of mechanical load.*

presented in (2.11) to (2.14). These can be applied directly to the drive equivalent model. As these expressions are function of the dc link rms voltage, all changes to circuit and system parameters before and including the dc link, (e.g. in the rectifier, supply system impedance, supply system voltage distortion, etc.) will be accounted for in this equivalent ASD model.

$$R_{eq(ct)} = 0.392V_{dc} + 0.316V_{dc}^2 - 0.51 \quad (2.11)$$

$$R_{eq(lt)} = 0.227V_{dc} + 0.323V_{dc}^2 - 0.167 \quad (2.12)$$

$$R_{eq(qt)} = 0.123V_{dc} + 0.320V_{dc}^2 + 0.084 \quad (2.13)$$

$$R_{eq(cp)} = 0.78V_{dc} + 0.267V_{dc}^2 - 1.144 \quad (2.14)$$

where: R_{eq} is in per-unit, ct, lt, qt, cp are denoting constant torque, linear torque, quadratic

torque, constant mechanical power loads, respectively, and V_{dc} is the per unit rms dc link voltage.

In order to validate the proposed model, comparisons were made between the full model and equivalent circuit model of the 4 kW open-loop V/Hz controlled ASD, for the four considered motor mechanical loading conditions, range of supply system voltages and dc link component values. The value of dc link components are selected as the minimum, nominal and maximum expected values and system impedance is set to nominal. Minimum value of L_{dc} is taken as zero, i.e. the ASD will be operating in discontinuous current conduction mode. In order to prevent repetition of similar results, Figure 2.39 shows the comparison for the ASD mechanically loaded with constant torque load, while the result for the other considered mechanical loading conditions may be found in Appendix A.3

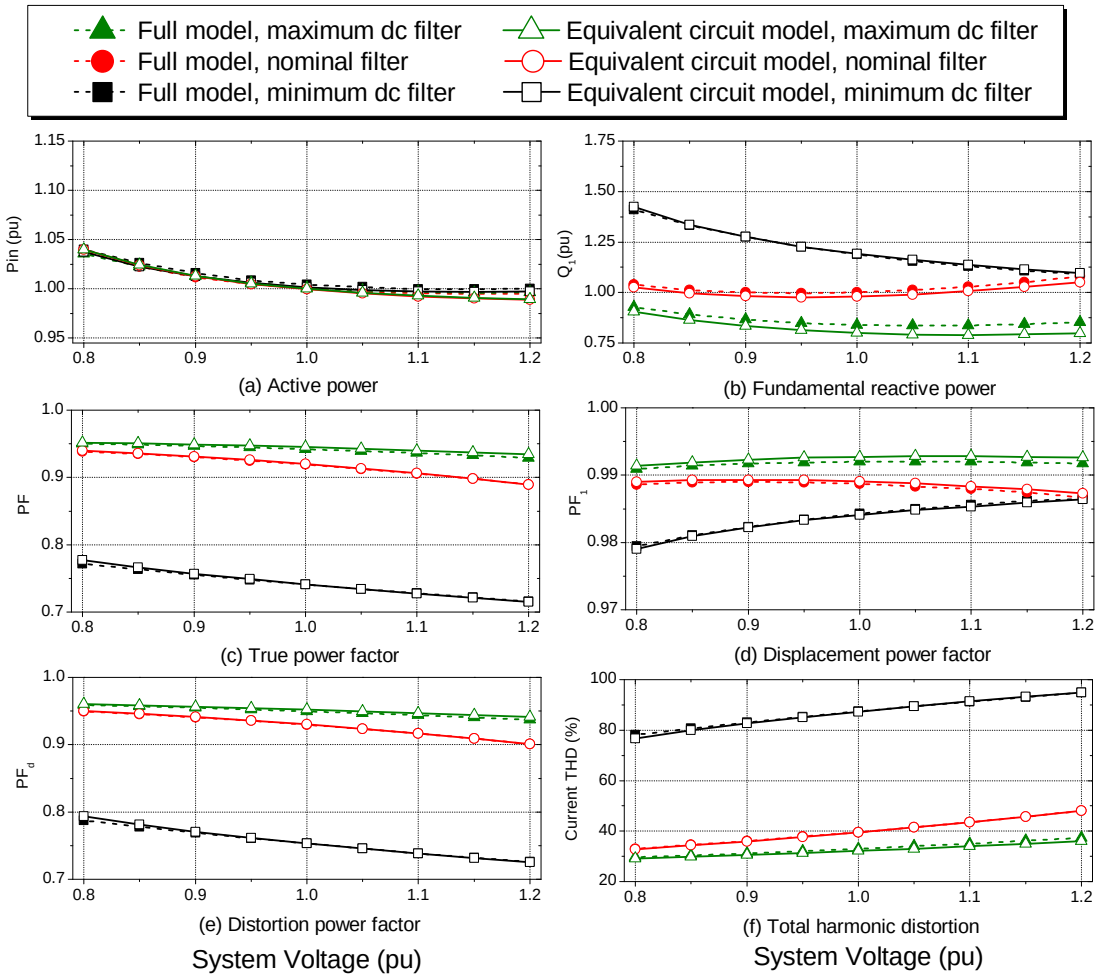


Figure 2.39: *Comparison between full model and equivalent circuit model for a range of dc link component values and motor loaded with constant torque load.*

The results in Figure 2.39 and Appendix A.3 show that the equivalent circuit model is able to accurately reproduce the active power demand characteristics of the full ASD model for all

four mechanical loading conditions, showing less than $\pm 2\%$ error across the considered system voltage range. The equivalent circuit model is also able to accurately predict non-active power demand characteristics, showing a less than $\pm 3\%$ error for PF, PF_1 and PF_d, for the four considered mechanical loading conditions and the range system voltage variation. Accordingly, the ability of the equivalent model to predict the fundamental reactive power is good, with maximum error no greater than $\pm 5\%$ across the considered ranges of values and parameters. Maximum error occurs at the ends of the considered voltage range.

The presented results, therefore, validate the equivalent model of the 4 kW open-loop V/Hz controlled ASD developed in this section. As only the active power characteristics of ASDs have been shown to change with the type of ASD, this equivalent model can also be used to represent all ASDs considered in this chapter. The representation of higher-power or advance controlled ASDs can be achieved by setting the equivalent ASD model resistance as a constant electrical power load, i.e as in (2.10), where P_{dc} is the dc link power which is essentially the same as the input power of the ASD as bridge rectifier losses will be small.

The developed equivalent model significantly reduces simulation run times, while retaining a good ability to predict ASD steady state active and non-active power demand characteristics. However, this equivalent circuit must be converted further to a form that can be readily aggregated. Such a model is developed in the next section.

2.11 Analytical model of ASD

The analysis in the previous section has shown that it is possible to considerably simplify the full ASD model, by reducing it to a three-phase rectifier, dc link and equivalent resistance. The equivalent circuit model developed in the previous section, although shown to be a very accurate representation of the full ASD, is somewhat cumbersome when aggregation of a number of ASD with other load types is required. Therefore, it would be far better to express this equivalent circuit model in an analytical form that can be written directly in computer code. This would enable a very flexible and modular approach to aggregation of ASD and other developed load models. In order to achieve this, the three-phase bridge rectifier should first be expressed analytically. References [66–69], all have discussed analytical models of three-phase drive controlled motors (from a harmonic analysis viewpoint), with [66] and [67] developing cumbersome, but full analytical expressions. However, other than the mentioned papers, there has been little work in this area. The remainder of this section focusses on developing an analytical model of ASDs. This model is developed in MatLab and referred to as ”analytical model”, as it uses a combination of differential equations and MatLab code to accurately represent the operation of the three-phase ASD.

As discussed in Section 2.2.1, the three-phase rectifier at the front-end of the ASD may be operated in discontinuous or continuous current conduction mode. Each mode of operation is initially considered separately in this section, with the two developed models subsequently combined.

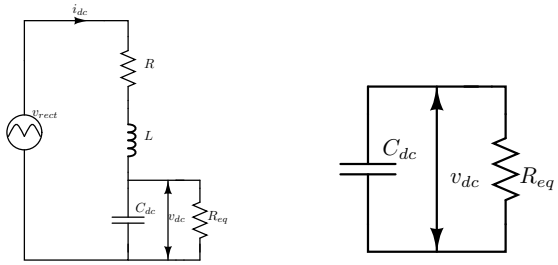
2.11.1 Analytical model: discontinuous current conduction mode

As explained in Section 2.2.1.1, the three-phase rectifier output voltage, v_{rect}, follows the envelope of the maximum line voltage. This voltage can be expressed by the analytical representation given in (2.15).

$$v_{rect} = maximum(|v_{ab}|, |v_{ac}|, |v_{bc}|) \tag{2.15}$$

Where: v_{ab}, v_{ac}, v_{bc} are instantaneous input line voltages.

As previously discussed, the phase current waveform, drawn by the three-phase rectifier in discontinuous current mode operation, can be broken down into two distinct subintervals: conduction and cut-off. In the conduction subinterval, two diodes will be conducting, and the dc link capacitor will be charging. The rectifier in this conduction period can be represented by the equivalent charging circuit, shown in Figure 2.40(a). When the dc link voltage is greater than v_{rect}, the three-phase rectifier will enter the cut-off period and C_{dc} will discharge. This cut-off period can be represented by the equivalent discharging circuit shown in Figure 2.40(b).



(a) Charging Circuit (b) Discharging Circuit

Figure 2.40: *Equivalent circuit representation of rectifier/capacitor charge and discharge states.*

The charge and discharge circuits shown in Figure 2.40 may also be expressed analytically by the following differential equations:

Charging:

$$v_{rect} = R \cdot i_{dc} + L \cdot \frac{di_{dc}}{dt} + v_{dc} \tag{2.16}$$

$$i_{dc} = C_{dc} \cdot \frac{dv_{dc}}{dt} + \frac{v_{dc}}{R_{eq}} \tag{2.17}$$

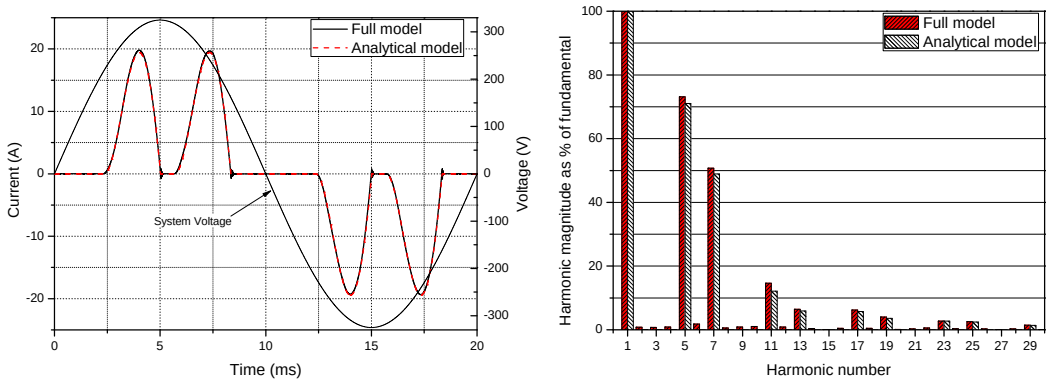
Discharging:

$$v_{dc} = v_{start} \cdot e^{\frac{-t}{R_{eq}C_{dc}}} \tag{2.18}$$

Where: L and R are the total inductance and resistance in the rectifier charging circuit conduction path. $L = L_{dc} + 2 \cdot L_{sys}$ and $R = 2 \cdot R_{sys} + 2 \cdot R_{diode}$ (current flows through two phases, i.e. L_{sys} and R_{sys} are therefore multiplied by two.), R_{eq} is the equivalent load resistance as developed in the previous section and C_{dc} is the dc link filter capacitor.

A MatLab code was developed to describe the operation of the three-phase rectifier in discontinuous current conduction mode. The code operates by comparing the value of v_{dc} to the value of v_{rect}. Based on this comparison, it solves either the charge or the discharge differential equation. The code is run in a loop with the simulation time iterated each time the loop is run. The value of v_{dc} at the end of each loop is passed to the beginning of the next loop. In this manner, both v_{dc} and i_{dc} are produced. This code can be found in Appendix A.4.

Figure 2.41 shows a comparison of the current waveforms and associated harmonics predicted by the developed analytical model and full model. The results show that the analytical model is able to almost perfectly match the current waveform and harmonic content of the full model. The results of comparison of P-V and N-V characteristics between the two models are shown and discussed later in Figure 2.48. The analytical model takes around 0.5 seconds to run a single ASD instance, compared to several minutes for the full ASD model. This is a significant reduction in simulation time, which is achieved with little loss in simulation accuracy.



(a) Current waveforms (b) Harmonics

Figure 2.41: *Comparison of input current waveforms and associated harmonics between full and analytical models of 4 kW open-loop V/Hz controlled ASD, loaded with constant torque mechanical load, operated in discontinuous mode, at 1pu system voltage.*

2.11.2 Analytical model: continuous current conduction mode

In order to produce an analytical model for continuous mode of operation, the two conduction subintervals (Section 2.2.1.2) must firstly be represented by analytical expressions based on equivalent circuits shown in Figure 2.43. During the conduction period, the voltage supplied to the RLC equivalent charge circuit, v_{cond} in Figure 2.43(a), will be the same as for the discontinuous situation, (v_{rect} in (2.15)). The values of the equivalent inductance and resistance will also be the same as for the discontinuous situation, i.e. $L = L_{dc} + 2 \cdot L_{sys}$ and $R = 2 \cdot R_{sys} + 2 \cdot R_{diode}$.

During the commutation period, two phases will conduct in parallel and one in series, as can be seen from Figure 2.42. Therefore, v_{comm} in Figure 2.43(b) can be expressed by (2.19). it can be seen from the conduction path that the values of L and R in the equivalent circuit will now be $L = L_{dc} + 1.5 \cdot L_{sys}$ and $R = 2 \cdot R_{sys} + 1.5 \cdot R_{diode}$.

$$v_{comm} = |v_b - \frac{v_a + v_c}{2} + v_{diode}| \tag{2.19}$$

Where: v_a, v_b, v_c are instantaneous system phase voltages and v_{diode} is the diode forward voltage drop.

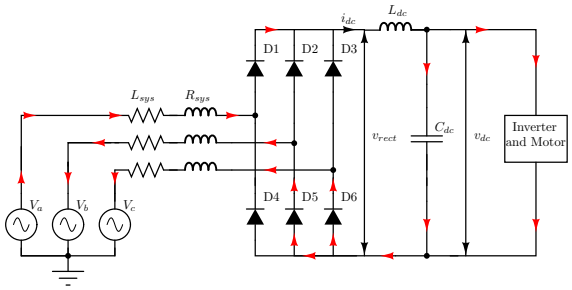


Figure 2.42: *Conduction path of rectifier during commutation period.*

(a) Conduction period (b) Commutation period

Figure 2.43: *Equivalent circuit representation of three-phase bridge rectifier operating in continuous mode.*

As before, MatLab is used to implement the analytical model of the three-phase rectifier operating in continuous current conduction mode. The operation of the developed code is summarised in a flow diagram, Figure 2.44. The steps will be explained in the following sections.

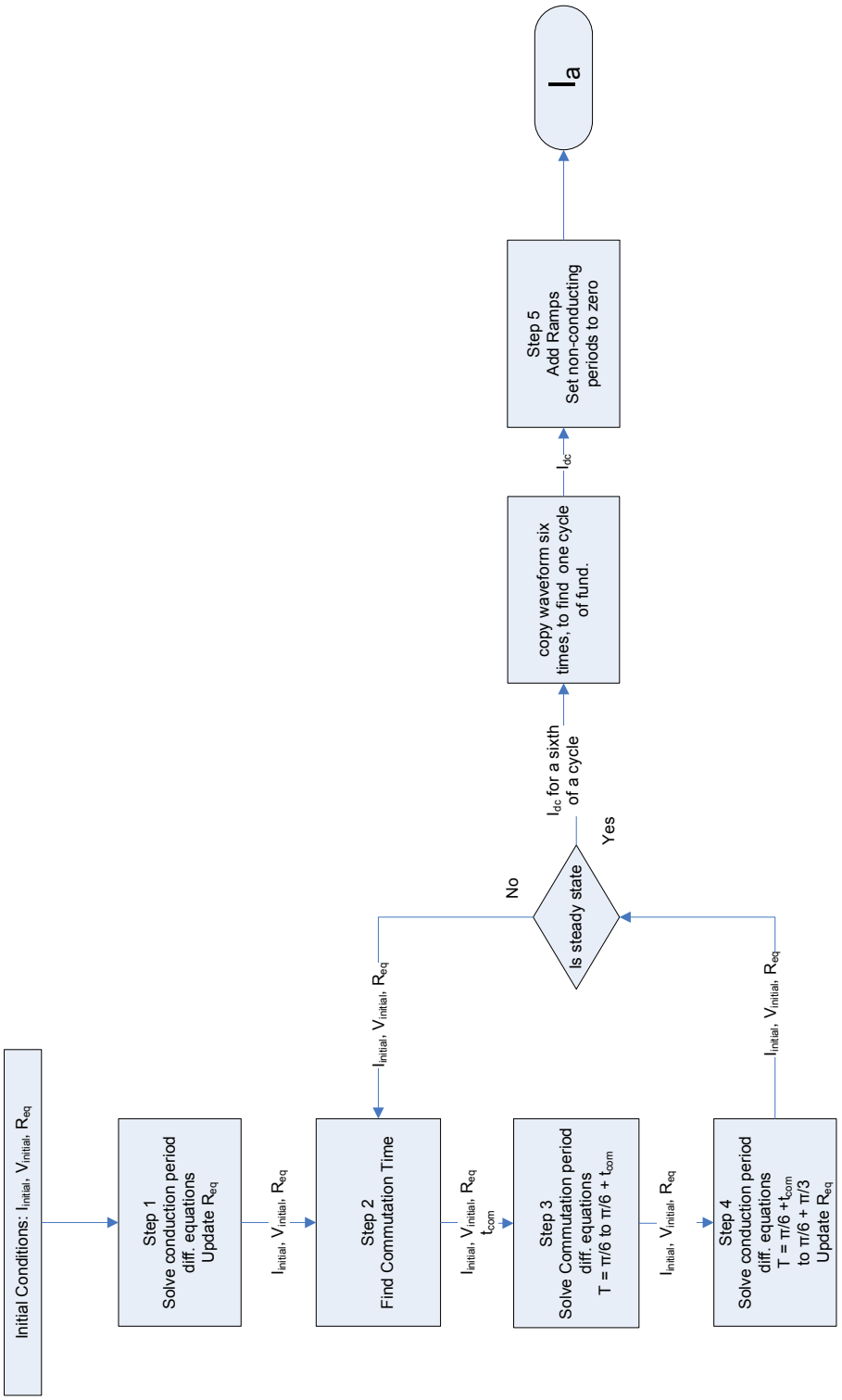


Figure 2.44: *Flow diagram of analytical model of three-phase rectifier operating in continuous current mode .*

2.11.2.1 Step 1: continuous RLC conduction circuit

The differential equations representing the conduction period of operation of the three-phase rectifier, (2.16) and (2.17), are solved in MatLab. This is done over several cycles of the fundamental system period to ensure steady state. This gives the voltage and current waveforms shown in Figure 2.45. The rms value of the voltage waveform, V_{dc}, is used to update the equivalent resistance from its initial condition, by employing the relevant equations (2.11) - (2.14).

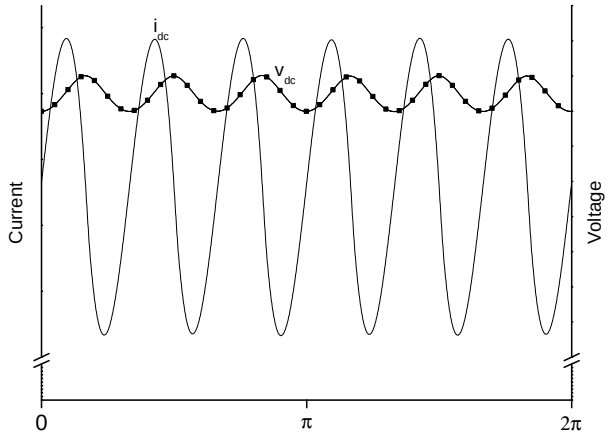


Figure 2.45: *Solution of differential equations representing three-phase rectifier conduction mode.*

2.11.2.2 Step 2: Commutation Time

As previously mentioned, the commutation time is the time taken by the relevant phase current, i_{phase}, to rise from zero to the magnitude of i_{dc}. The system impedance forms an RL circuit during the commutation periods. The effective voltage applied to this circuit, v_{ramp}, is the difference between the relevant line and rectifier commutation voltage. For example, if considering phase A as the reference point, the applied voltage to the RL charging circuit is:

$$v_{ramp} = v_{ab} - |v_b - \frac{v_a + v_c}{2} + V_{diode}| \tag{2.20}$$

Where: v_{ab} is instantaneous input line voltage.

The analytical expression for this circuit is:

$$i_{ramp} = \frac{v_{ramp}}{2R_{sys}} * (1 - \exp^{\frac{-t*R_{sys}}{L_{sys}}}) \tag{2.21}$$

The time that the current i_{ramp} takes to reach i_{dc} will be the commutation time t_{com}, as illustrated in Figure 2.46.

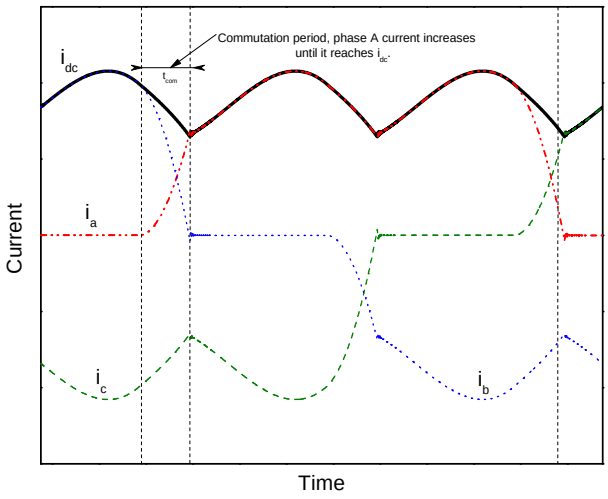


Figure 2.46: *Commutation and conduction period current waveforms.*

2.11.2.3 Steps 3-4: Commutation period and iteration

The differential equations representing the commutation subinterval are now solved, for the period of commutation, t_{com}, found in the previous step and starting from the beginning of the commutation interval, ($t = \frac{\pi}{6}$). The voltage and current from step one at the start point of the commutation period are used as initial conditions of the differential equations. Thus, the dc link commutation current and voltage waveforms are produced for the commutation time. At the end of the commutation period, the dc link current and voltage can be used as initial conditions for the conduction period differential equations, and steps 1-3 can be run in a loop until steady state operation is achieved.

2.11.2.4 Step 5: Convert i_{dc} to i_a

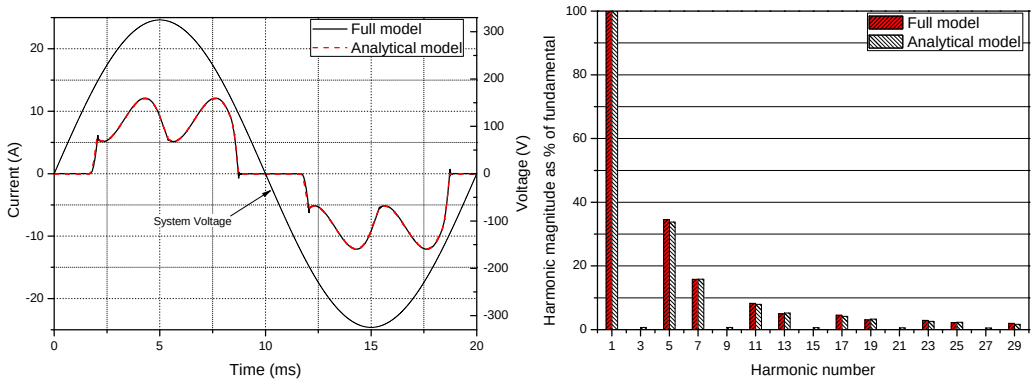
Once the final i_{dc} current waveform has been found, it must be converted to a phase input current. As can be seen from Figure 2.46, the conduction period of each phase current will follow the envelope of i_{dc} for the period that this phase is conducting. The 'ramp-up' current, when the relevant phase starts to conduct, has already been discussed. The 'ramp-down' current is simply the reciprocal of the 'ramp-up' current. The differential equation representing the 'ramp-down' current can be expressed as in (2.22). These current ramps may now be added to the relevant part of the i_{dc} current waveform, with the non-conduction sections being set to zero to give the input phase current.

$$i_{rampdown} = i_{start} - \frac{v_{ramp}}{2R_{sys}} * (1 - e^{\frac{-t*R_{sys}}{L_{sys}}}) \tag{2.22}$$

where i_{start} is the start point of the discharge ramp, i.e the dc link current at the end of the commutation period.

The above procedure was implemented in MatLab code to give an analytical representation of the three-phase rectifier in continuous mode, and this code may be found in Appendix A.4.

Figure 2.47 show a comparison between the input current and associated harmonics, at 1pu system voltage, of the full and analytical models, for the ASD operating in continuous conduction mode. It can be seen from this figure that the current waveforms of the analytical model can accurately match the actual current waveform of the full model. The results for harmonics demonstrate that this developed model can also be used for harmonic analysis.



(a) Current waveforms (b) Harmonics

Figure 2.47: *Comparison of input current waveforms and associated harmonics between full and analytical models of 4 kW open-loop V/Hz controlled ASD, loaded with constant torque mechanical load, operated in continuous mode, at 1pu system voltage.*

2.12 Validation of analytical ASD model for sinusoidal and non-sinusoidal conditions

The P-V and N-V characteristics predicted by the developed analytical ASD model are now compared with those of the full ASD model. Initially, sinusoidal voltage is applied to both models. After verification of the analytical model in sinusoidal situations, comparisons are made between the two for applied non-sinusoidal voltage waveforms. In all cases, a 4 kW V/Hz open-loop controlled ASD is selected, with analysis performed for minimum, nominal and maximum values of dc link components and nominal value of system impedance. The result presented in the main text are for 4 kW ASD mechanically loaded with constant torque. The results for 4 kW ASD mechanically loaded with the other considered torques and for applied sinusoidal voltage can be found in Appendix A.5.

2.12.1 Sinusoidal voltage supply conditions

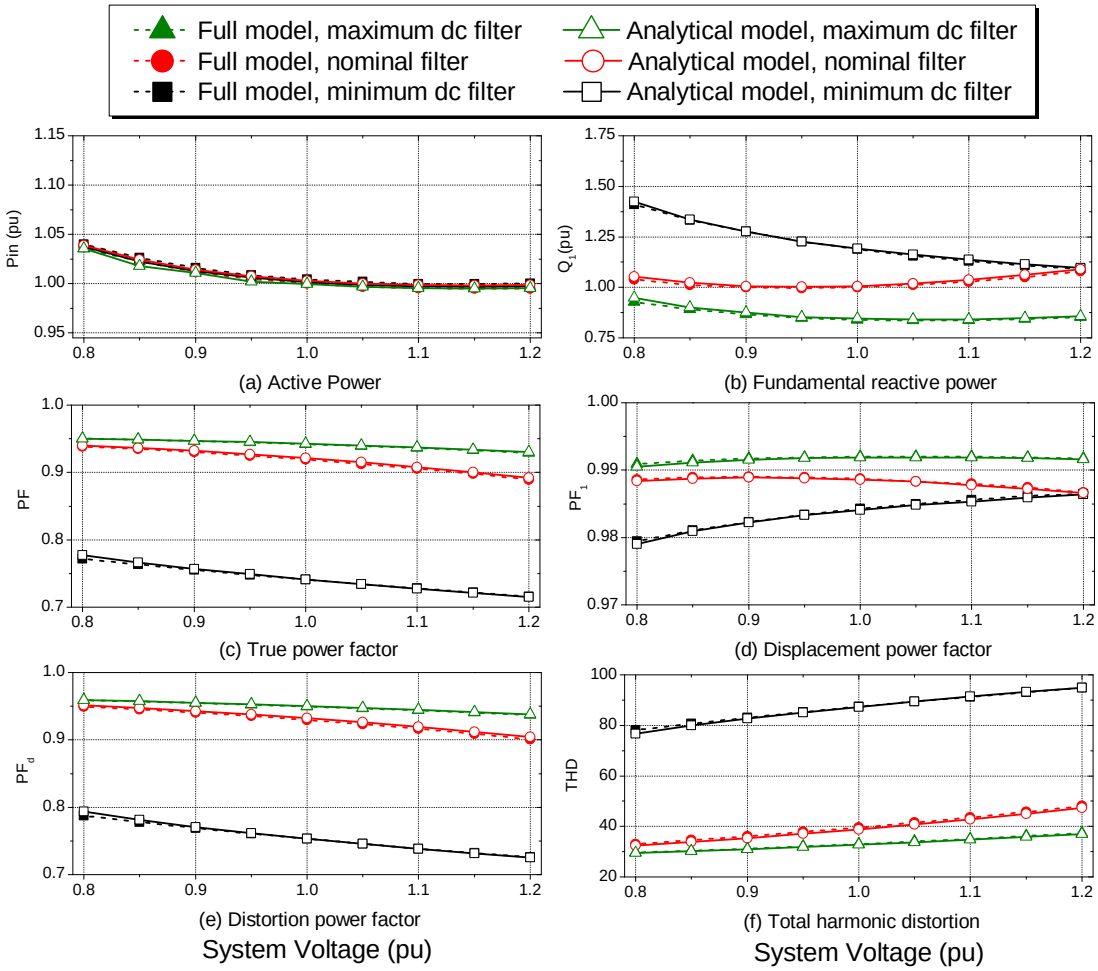


Figure 2.48: *Comparison between full and analytical ASD models for a range of dc link component values and motor loaded with constant torque load.*

Figure 2.48 shows the results of the comparison between the full and analytical models for applied sinusoidal system voltage. It can be see from this figure that the analytical model shows excellent matching for all considered active and non-active power characteristics. Thus, this result validates the developed analytical model for use in sinusoidal situations.

2.12.2 ASD supplied with non-sinusoidal voltage

The modern UK supply system voltage is rarely sinusoidal, due to the presence of non-linear loads. Therefore, ASDs will in all probability be supplied with distorted voltage, and developed analytical ASD model should also be validated under these supply conditions. In order to obtain a "typically distorted" distribution system voltage waveform to use in the following analysis, the system voltage was measured at three locations. Each location represents a different type of distribution network.

Commercial supply voltage The University of Edinburgh power lab voltage was measured at 11am on a weekday during term time. This lab is located on a large campus with large numbers of fluorescent lighting, PCs, monitors and other non-linear loads.

Urban supply voltage The voltage waveform from a flat in a residential part of Edinburgh was measured at 11am on a typical weekday. The flat is in a block of 16 flats in a large residential area, consisting mainly of small flats.

Rural supply voltage The system voltage was also measured at 11am on a typical weekday in a small rural village in the Brecon Beacons national park, South Wales.

Each of the measured voltage waveforms are shown in Figure 2.49. It can be seen that these waveforms are all similar in shape and have similar values of voltage THD. This result is somewhat surprising, as it was expected that the measured rural voltage would be less distorted than the urban and commercial measured voltages. However, due to the little difference between the measured voltages, the University lab voltage is taken as a "typical" distribution system voltage. This waveform is referred to as "typically distorted" waveform for the remainder of this thesis. In order for the models to be tested under more distorted supply conditions, and to provide further validation, an artificially distorted system voltage was constructed. This waveform has an 8% THD, made mostly from the 3^{rd} harmonic, and referred to as "heavily distorted" waveform in the remainder of this thesis.

The "typically distorted" and "heavily distorted" waveforms were applied to the full and analytical ASDs models, with the results shown in Figures 2.50 to 2.55.

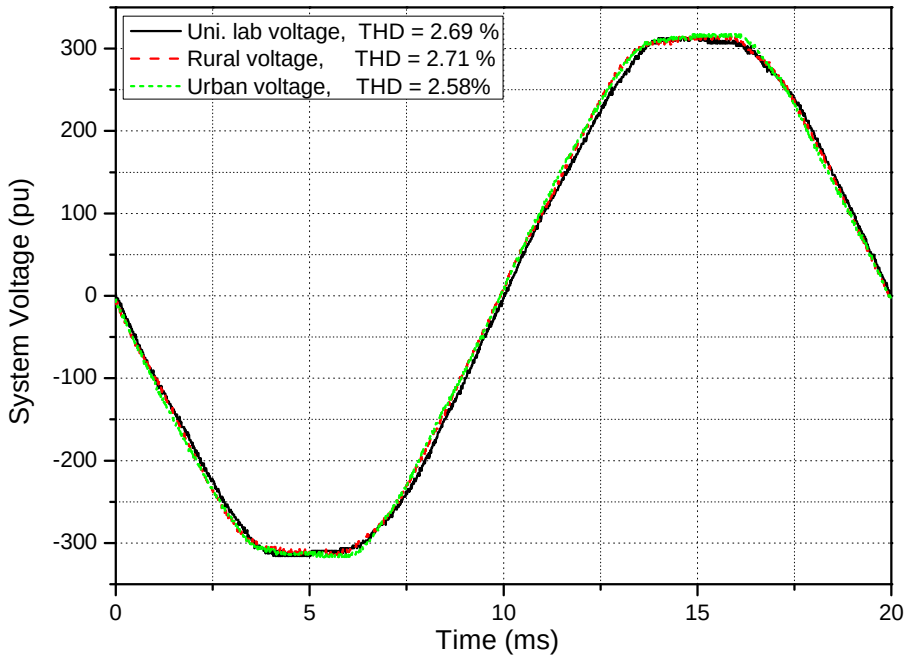
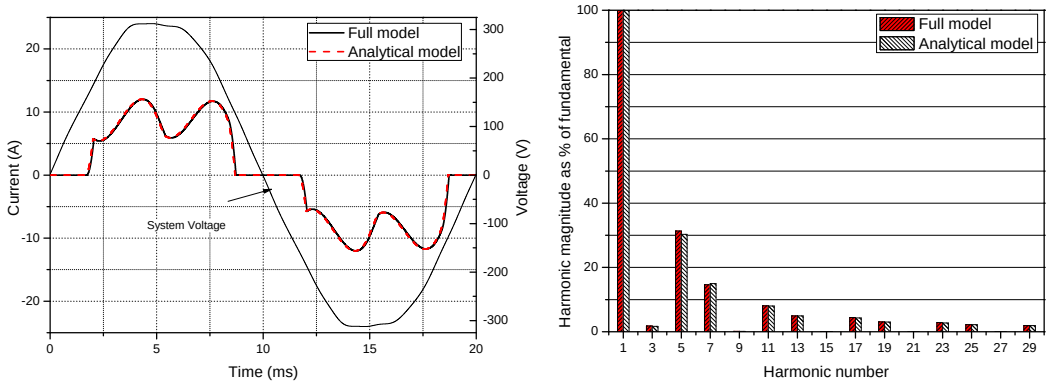
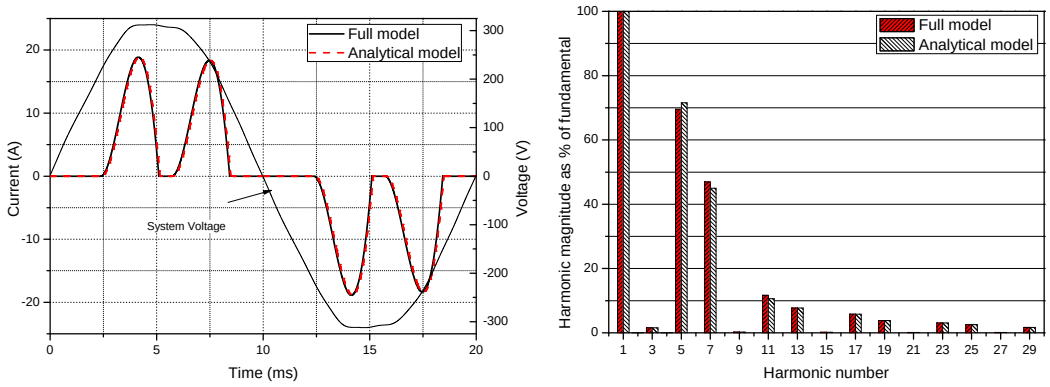


Figure 2.49: *System voltage waveforms measured in commercial, urban and rural areas.*



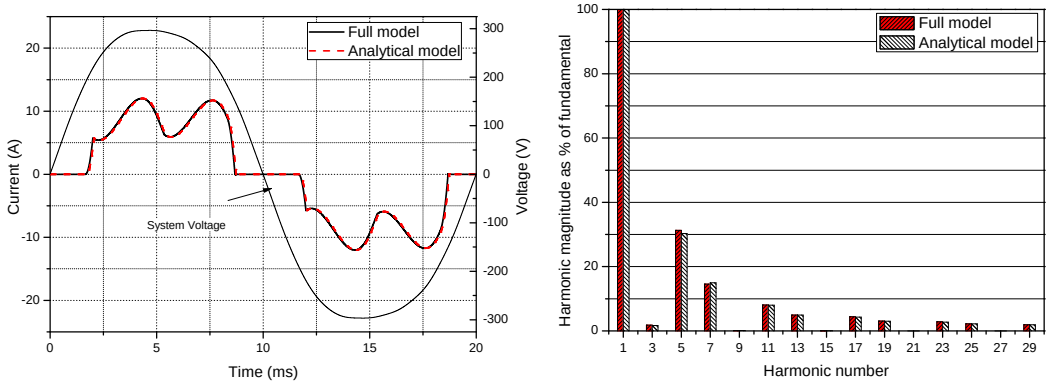
(a) Current waveforms (b) Harmonics

Figure 2.50: *Comparison between full and analytical model, with applied 1pu "typically distorted" system voltage, ASD in continuous mode.*



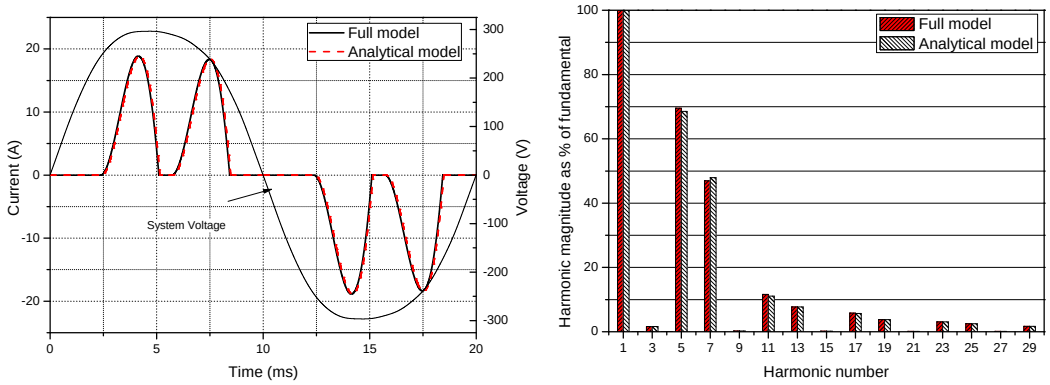
(a) Current waveforms (b) Harmonics

Figure 2.51: *Comparison between full and analytical model, with applied 1pu "typically distorted" system voltage, ASD in discontinuous mode.*



(a) Current waveforms (b) Harmonics

Figure 2.52: *Comparison between full and analytical model, with applied 1pu "heavily distorted" system voltage, ASD in continuous mode.*



(a) Current waveforms (b) Harmonics

Figure 2.53: *Comparison between full and analytical model, with applied 1pu "heavily distorted" system voltage, ASD in discontinuous mode.*

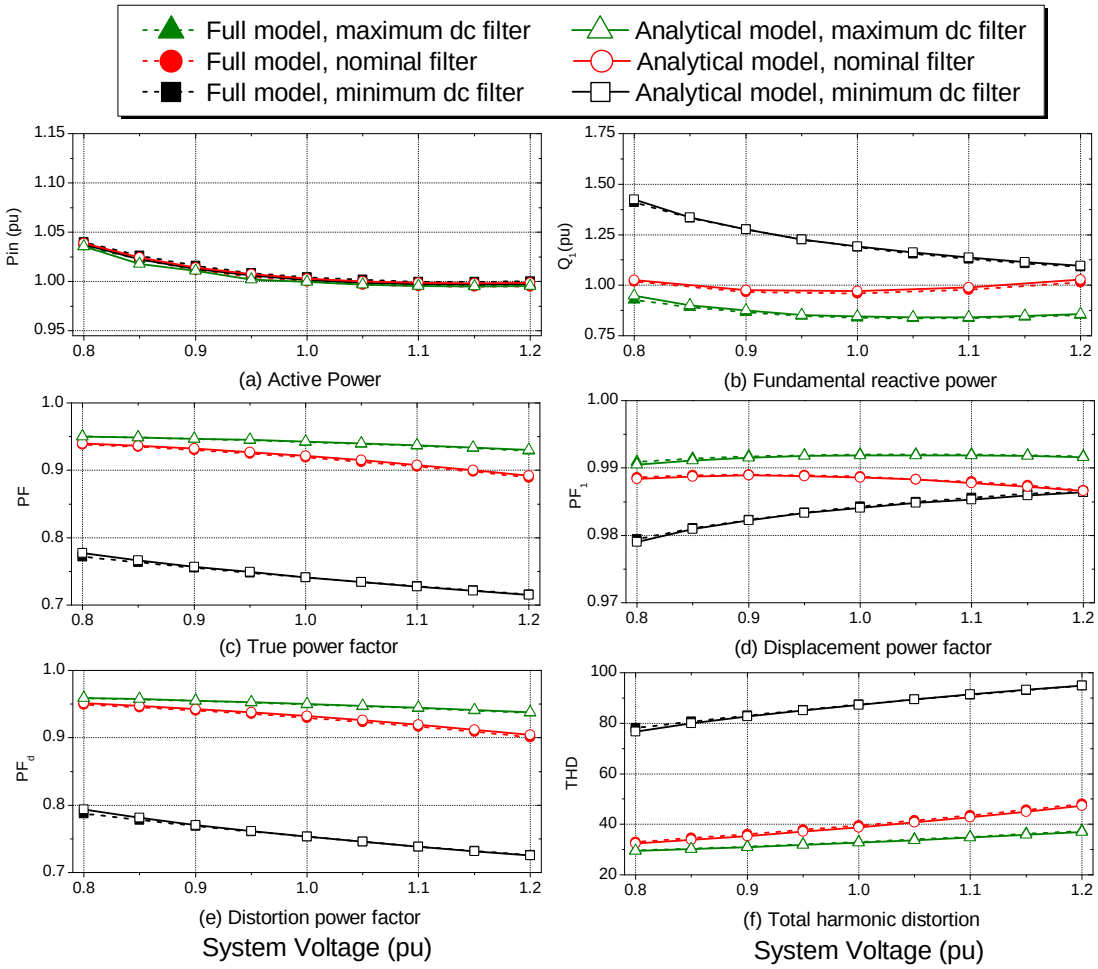


Figure 2.54: *Comparison between full and analytical models for a range of dc link component values, motor loaded with constant torque load and applied "typically distorted" system voltage.*

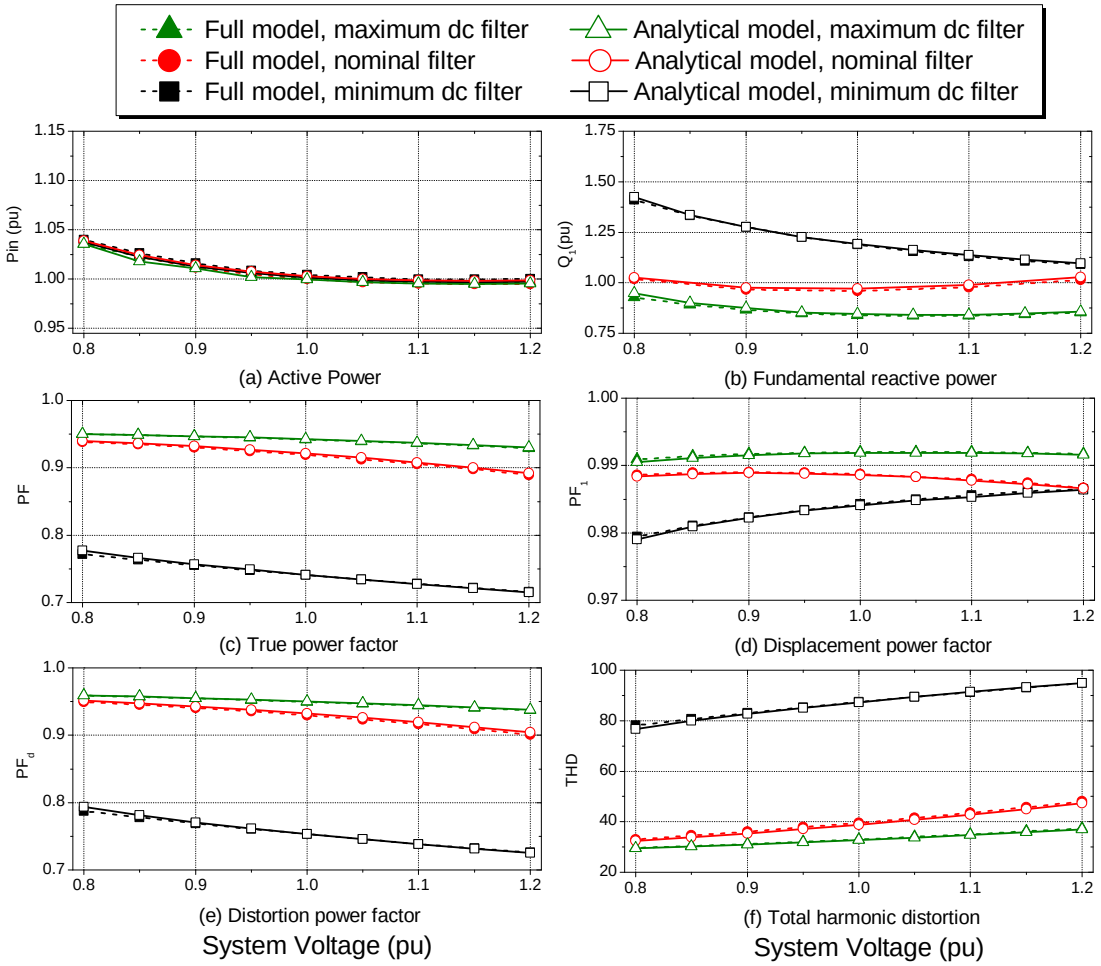


Figure 2.55: *Comparison between full and analytical models for a range of dc link component values, motor loaded with constant torque load and applied heavily distorted system voltage.*

It can be seen from the presented results that for considered distortions in the system voltage the proposed analytical model can very accurately represent relevant ASD characteristics.

2.13 Generic analytical model of ASDs

From the work presented so far in this chapter, it can be seen that there will be two general sub-types of ASD load: ASD operating in continuous mode and ASD operating in discontinuous mode. Within each sub-type, there will be six further possible variants, which depend on the type of motor mechanical loading, the rated power of the ASD and the method of drive control. Although the P-V characteristics of each of these variants will be different, it has been shown that if their P-V characteristics and values of dc link filter components are known, the developed analytical model may accurately predict N-V and harmonic characteristics of

these loads. Thus, as the P-V characteristics have been determined in Section 2.8, all that is required to form generic models of typical ASDs is typical values of their dc link components. These values have already been presented in Section 2.4.

Accordingly, to represent the ASD operating in continuous mode, nominal per-unit values of L_{dc} and C_{dc} can be selected from Section 2.4. To represent the ASD operating in discontinuous mode, L_{dc} should be set to zero and C_{dc} should be taken as nominal. As the values of C_{dc} and, where relevant L_{dc}, have already been presented in per-unit, the associated generic models of each sub-type variant may be used to represent the general characteristics of an aggregate of considered type of ASD load. It is should be noted that this representation assumes that all ASDs within a considered sub-type will have the same per-unit value of C_{dc} and, where relevant L_{dc} and will also all operate at nominal rated power. It may be the case that diversity in the same sub-type of ASD load, i.e. variation in the ASD parameters and operating powers, could affect the harmonic content of an aggregate load, an effect known as harmonic cancellation. However, this effect is not expected to be significant for this load type. Another parameter that will also affect the developed generic load models, and that can not be taken as a typical per-unit value, is the system impedance. However, it has been shown that variations of system impedance within a typical range will have only slight effect on ASD characteristics.

The proposed generic model may be achieved, as harmonic legislation does not directly interfere with the design of ASDs. Therefore, these loads may be expressed readily in per-unit form, which is common to all ASD loads, irrespective of the rated power of the ASD. This is not the case for other non-linear loads considered in the following chapters. Also, it is not possible to define a generic ASD load mix. This is because these loads are used in a wide range of applications, with the type and size of ASDs used dependent on the application. However, by presenting generic analytical ASD models of a wide range of ASD types and rated powers, flexibility to represent the vast majority of ASDs in load mixes has been provided.

2.14 Polynomial and exponential models of ASDs

For the completeness of the analysis, polynomial and exponential interpretations of the generic analytical ASDs model coefficients have also been developed and are presented in Table 2.8. This table also compares ASD model coefficients with those previously derived for directly-connected motors. Although these models take no account of ASD harmonic characteristics, they may be used as basic models of the ASD loads in standard load flow analysis. From the results and discussion in Section 2.12.2, it has also been shown that these models will be valid in non-sinusoidal situations.

Figures 2.56 and 2.57 show plots of the derived exponential and polynomial models for

V/Hz open-loop operated lower-power ASDs operated in continuous mode, compared with the analytical model. Again, it can be seen that the presented polynomial models will show better matching than the exponential models, especially for fundamental reactive power characteristics. The few available previous polynomial and exponential models of ASDs are shown in Table 2.4, [22] and also plotted in Figures 2.56 and 2.57. These previous ASD models, according to [22], are of rated power of 2 kW, and hence they are compared with the developed lower-power ASD models. Considerable disagreement can be seen between the previously developed ASD models and the proposed ASD models. There was no information given in [22] as to the type, operating mode or mechanical loading condition of the ASDs used to derive the previous exponential and polynomial load models. Due to this lack of data, it is difficult to make any further comment other than that the ASDs represented in [22] have very strange P-V characteristics, as they act as near constant current loads, which is contrary to work presented in this thesis (and other previous work related to directly connected motors, which should have similar P-V characteristics to ASDs).

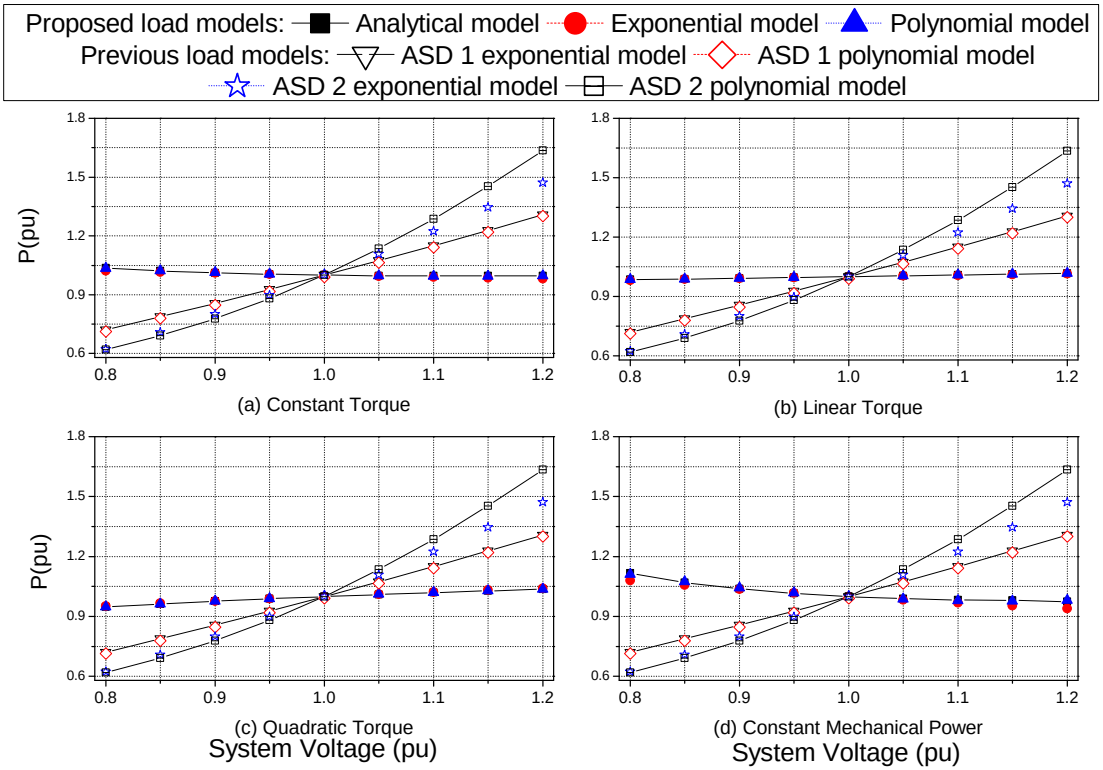


Figure 2.56: *Results obtained using proposed exponential and polynomial models of lower power ASDs, compared with results obtained from previous models, active power.*

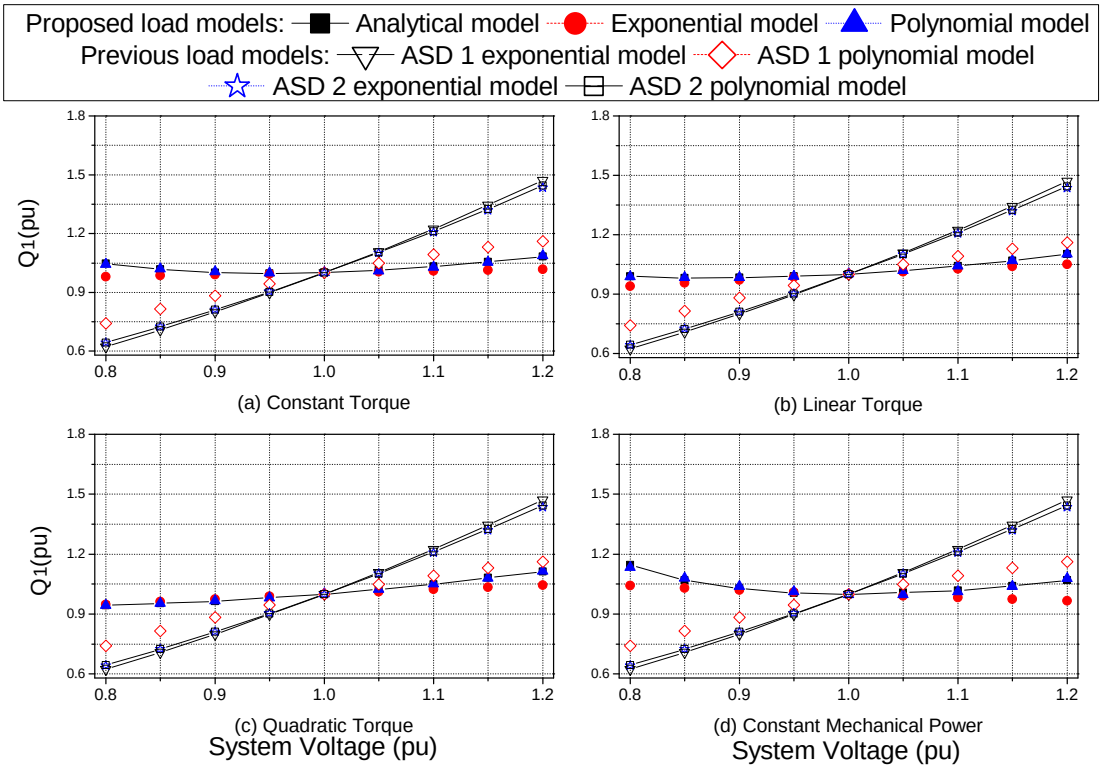


Figure 2.57: *Results obtained using proposed exponential and polynomial models of lower power ASDs, compared with results obtained from previous models, fundamental reactive power.*

Table 2.8: *Proposed exponential and polynomial model coefficients for ASDs operated in discontinuous and continuous modes compared with exponential and polynomial model coefficients of directly connected motors, (as previously presented).*

Loading	ASD model parameters									Directly connected motor model parameters								
	PF_1	Exp. Model		polynomial Model						PF_1	Exp. Model		polynomial Model					
		np	nq	Z_p	I_p	P_p	Z_q	I_q	P_q		np	nq	Z_p	I_p	P_p	Z_q	I_q	P_q
DISCONTINUOUS MODE OF OPERATION Lower power V/Hz open-loop ASDs										Lower power directly connected								
CT	0.984	-0.10	0.09	0.40	-0.89	1.49	1.60	-3.10	2.50	0.83	-0.1	1.44	0.27	-0.63	1.36	1.55	-1.7	1.15
LT	0.984	0.08	0.28	0.02	0	0.98	1.10	-1.91	1.81	0.83	0.02	1.44	0.02	-0.02	1.0	1.55	-1.7	1.15
QT	0.984	0.22	0.24	-0.27	0.76	0.51	0.70	-0.98	1.28	0.83	0.13	1.44	-0.15	0.43	0.72	1.55	-1.7	1.15
CP	0.984	-0.19	-0.98	1.08	-2.5	2.42	2.67	-5.49	3.81	0.83	-0.25	1.44	0.64	-1.53	1.89	1.55	-1.7	1.15
Lower power V/Hz closed-loop ASDs										not applicable								
all	0.984	-0.35	-0.28	1.08	-2.5	2.42	2.51	-5.96	4.45	not applicable								
Higher power V/Hz open-loop and closed-loop ASDs										Higher power directly connected motors								
all	0.984	-0.07	-0.3	0.13	-0.33	1.20	0.55	-1.7	2.15	0.9	-0.01	1.13	0.03	-0.06	1.04	1.60	-2.10	1.5
Lower and higher power V/Hz ASDs with advanced control										not applicable								
all	0.984	0	-0.5	0	0	1	1.22	0.45	-0.67	not applicable								
CONTINUOUS MODE OF OPERATION Lower power V/Hz open-loop ASDs										Lower power directly connected								
CT	0.989	-0.17	-0.08	0.45	-1.07	1.62	1.75	-3.55	2.8	0.83	-0.1	1.44	0.27	-0.63	1.36	1.55	-1.7	1.15
LT	0.989	0.04	0.17	0.02	0	0.98	1.18	-2.18	2.0	0.83	0.02	1.44	0.02	-0.02	1.0	1.55	-1.7	1.15
QT	0.989	0.22	0.35	-0.27	0.76	0.51	0.66	-0.97	1.31	0.83	0.13	1.44	-0.15	0.43	0.72	1.55	-1.7	1.15
CP	0.989	-0.35	-0.28	1.08	-2.5	2.42	2.64	-5.5	3.9	0.83	-0.25	1.44	0.64	-1.53	1.89	1.55	-1.7	1.15
Lower power V/Hz closed-loop ASDs										not applicable								
all	0.989	-0.35	-0.28	1.08	-2.5	2.42	2.64	-5.5	3.9	not applicable								
Higher power V/Hz open-loop and closed-loop ASDs										Higher power directly connected motors								
all	0.989	-0.07	0.20	0.13	-0.33	1.20	1.30	-2.38	2.08	0.9	-0.01	1.13	0.03	-0.06	1.04	1.60	-2.10	1.5
Lower and higher power V/Hz ASDs with advanced control										not applicable								
all	0.989	0	0	0	0	1	0.99	-1.96	1.97	not applicable								

2.15 Conclusions

This chapter presents analysis of the steady state active/non-active power demand characteristics of directly connected and drive-controlled three-phase induction motors. Detailed simulation models of each of these load types have been developed and verified.

It has been shown that there is a clear distinction between active power demand characteristics of lower-power ($\leq$ 15 kW) and higher-power (15 kW-160 kW) directly connected motors, while reactive power demand characteristics of these two types of motors are more similar. It has further been shown that a single polynomial/exponential models may be used to represent accurately each of the P-V and Q-V characteristics of higher-power motors. One Q-V characteristic and four separate polynomial/exponential models are required for correct representation of lower-power motor P-V characteristics. This is because the P-V characteristics of lower-power motors are strongly influenced by the type of motor mechanical load. Developed polynomial and exponential models of higher-power motors have been compared with existing models found in literature, and have been found to be generally in good agreement. However, there is a lack of literature with regards to steady state load models of lower-power motors loaded with different types of mechanical load, hence part of the reason for this work. The developed load models of lower and higher power directly connected three-phase motors are presented in standard polynomial/exponential forms that may be used directly in power system analysis. As the models have been developed based on type of motor mechanical loading conditions, rather than on specific motor applications, they provide the flexibility to represent any common type of mixed aggregate directly connected three-phase motor load.

The active power, non-active power and harmonic characteristics of currently used and future types of drive-controlled three-phase motors (ASDs) have been investigated. It has been shown from the presented analysis that the currently common V/Hz controlled open-loop ASDs have similar P-V characteristics to those of directly connected motors. Higher-power V/Hz controlled open-loop ASDs show little variation in P-V characteristics with applied motor mechanical loading condition, while influence of mechanical load is fairly significant on the P-V characteristics of lower-power V/Hz controlled open-loop ASDs. Both lower and higher power ASDs that employ V/Hz closed-loop control may be represented as V/Hz open-loop controlled ASDs loaded with constant power mechanical load. ASDs with advanced control (e.g. vector control), which are expected to increase in numbers over the next years, will have constant P-V characteristics.

The non-active and harmonic characteristics of ASDs have been shown to be influenced by the mechanical loading of the ASD, the values of dc link components and, to a lesser extent, the system impedance. It has been shown that, based on the values of dc link components, ASDs

will operate in one of two distinctive modes: continuous or discontinuous, with each mode of operation having significantly different non-active power demand and harmonic characteristics. In order to represent non-active and harmonic characteristics of ASDs, an analytical model of this load has been developed and verified for both sinusoidal and non-sinusoidal supply conditions. Research into the typical value of ASDs dc link filter components has been performed, as well as an investigation into harmonic legislation relevant to these loads. From this work, it is not expected that current harmonic legislation will have significant effect on the selection of ASD dc link filter components.

Combining the developed analytical ASD model with the knowledge of typical dc link filter components and P-V characteristics of the considered types of ASDs, allowed for the development of generic analytical models of these load types. The developed generic analytical models are able to accurately represented all active power, non-active power and harmonic characteristics for the considered types of ASDs. These models may be used directly to form aggregate loads of a desired mix of ASD loads, or used directly as aggregate models themselves if the aggregate load to be modelled is made up of the same type of ASD load. Thus, the developed loads generic ASD models are extremely versatile. Polynomial and exponential interpretations (i.e models) of the generic analytical ASD models have been also presented. These two models may be used to represent P-V and Q_1-V characteristics in load flow analysis, but cannot be used for more detailed analysis of ASDs provided by analytical models (e.g. non-active and harmonic characteristics).

It is important to note that ASDs in both continuous and discontinuous modes of operation have close to unity displacement power factors. Therefore they will not contribute significantly to reactive power flow in the supply system. This means that the expected future transition from directly connected to drive-controlled three-phase motors will have a large effect on the fundamental reactive power flow in the supply system, as directly connected motors operate with much lower power factors. Accordingly, the main issues related to increased amounts of ASD loads in the future are increased harmonics in the supply system and the corresponding adverse effects on system voltage quality. Hence the reason for the requirement for developed analytical models to fully represent the harmonic characteristics of these load types under both sinusoidal and non-sinusoidal conditions. Accordingly, the proposed models are fully suitable for further investigation of all implications of the expected future increased penetration of ASD loads.

Chapter 3
Single-phase directly connected and drive-controlled induction motors

3.1 Introduction

Single-phase induction motors (SPIM) are the most commonly used type of ac motors in the world. It is estimated that there are around 100 million SPIMs in the UK alone, accounting for over 3% of the total energy consumption due to all motor loads, [43] and [70]. These motors are mainly used in domestic/residential applications, where they make up around 16% of the total domestics demand, [43]. Typical applications with these motors include refrigerators, chest/upright freezers, fridge-freezers, household air conditioners, fans, pumps and other motor-driven electrical equipment. Table 3.1 gives the typical rated power of 'cold appliances' in the UK, as well as the estimated contributions of each appliance to the total power consumption in this load category, [71].

Table 3.1: *Cold appliances in UK households in 2008, [71].*

Appliance	Unit rated power demand (W)	Total rated power demand (GW)	Contribution %
Chest-Freezer	100	0.42	4.9
Fridge-Freezer	230	3.9	45
Refrigerator	230	2.6	30
Upright Freezers	230	1.7	19.7

At present, directly connected SPIMs are almost exclusively used in both low power applications, such as domestic fridge/frezers (less than $\frac{1}{4}$hp), and higher power applications (around 1hp), such as air conditioners. There is currently considerable interest in replacing some of these motors with single-phase adjustable speed drives (SASDs). The main reasons behind this substitution are: the requirements for better speed and performance control, and concerns for improved energy efficiency. This trend is especially apparent in air conditioning applications, where it is estimated that an energy saving of 13% may be achieved yearly by using a SASD instead of a SPIM [72]. This is because SASD can operate at variable speed to keep the temperature constant, avoiding start-up and run-down losses incurred in a directly connected SPIM, due to numerous switch-on and switch-off periods. Furthermore, until recently, washing machines, which account for around 4% of the total domestic demand, have mainly been driven by so called 'universal motors'. However, the next generation of washing

machines, which are currently being produced, are expected to employ SASD, [73]. It is estimated that currently 37% of traditionally SPIM applications in Japan use SASD, with 86% of air conditioners using SASD [74], [75].

Existing literature provides some guidance on the load modelling and representation of directly connected single-phase motors, suggesting a few exponential models of these load types, Table 3.2. There is no guidance on how to represent SASD in power system studies in previously published literature. In order to address this gap, and to estimate the extent of the expected changes in the characteristics of the future loads, this chapter compares steady state load characteristics (e.g. active and reactive/non-active power demand) of directly connected single-phase induction motors and SASDs. It is shown that SPIMs may be represented using polynomial and exponential models, with such models being developed and presented. However, the analysis in this chapter shows that the non-active power and harmonic characteristics of SASD require a more detailed model, due to the non-linear operation of this load. Therefore, an analytical model of SASD load is developed and validated. It is shown that this analytical model is able to represent the non-active and harmonic characteristics of SASDs for both sinusoidal and non-sinusoidal situations. From the analysis and discussions of typical component values found in SASDs and harmonic limits applicable to these loads, it is found that there are two distinctive sub-types of SASD load. While active power demand characteristics of each sub-type of SASD load are similar, non-active power and harmonic characteristics will be significantly different. Generic analytical load models are developed for each of these SASD sub-types of load, with these generic models used later in the thesis to represent an aggregation of the same sub-type SASD load. Finally, exponential and polynomial interpretations of these generic analytical SASD models are presented.

Table 3.2: *Existing load model coefficients for directly connected single-phase motors.*

Motor Type	Power factor	Exponential model coefficients		Source
		n_p	n_q	
Clothes washer	0.65	0.08	1.6	[19]
Refrigerator	0.8	0.77	2.5	[15]
1-phase air con.	0.96	0.202	2.3	[15]

3.1.1 Motor mechanical loading

As discussed in Section 2.1.1, there are four general types of motor mechanical loads, likely to be found in motor applications: constant torque, linear torque, quadratic torque and constant mechanical power. When considering likely mechanical loading applied to a SPIM, typical

SPIM applications should be considered. These applications can be roughly divided between ”cold”, ”wet” and ”standard” motor applications. Types of mechanical loading associated with each of these applications are discussed below.

Wet appliances Examples of these loads include: dishwashers, washing machines, tumble driers and washer driers. The SPIM found in these appliances will be used for rotation of the machine 'drum'. As the mass of the drum and its contents do not change with motor speed, the mechanical loading on the SPIM is expected to be constant torque type.

Cold appliances Examples of these loads include: refrigerators, chest/upright freezers, fridge-freezers and household air conditioners. All these appliances operate on the principle of compression and then expansion of a coolant. The compression is achieved usually with a rotatory compressor driven by a SPIM, which operates as a quadratic torque load mechanical load, [76].

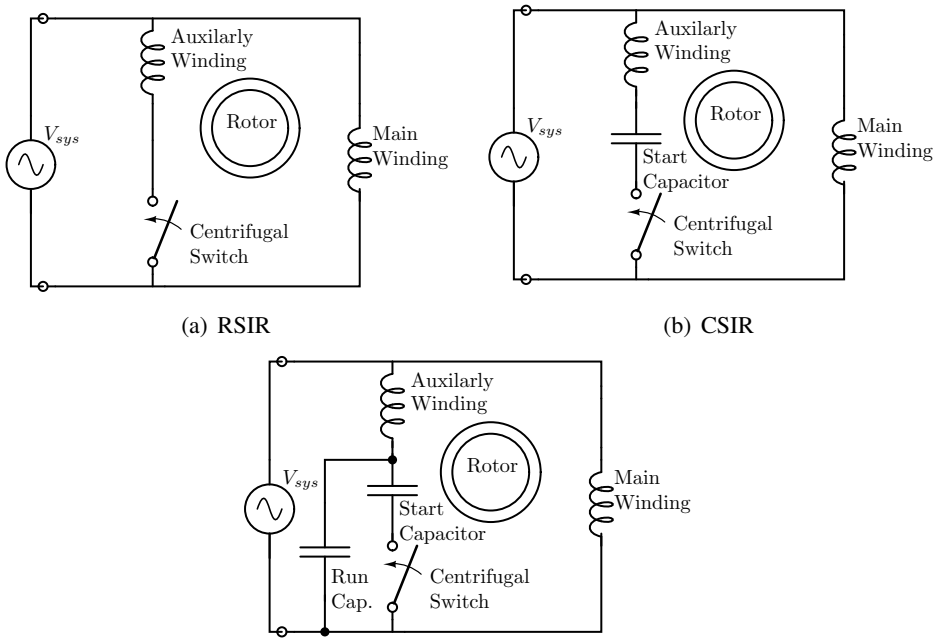
Standard motor applications Examples of these loads include: fans, pumps and other motor-driven electrical equipment. Centrifugal pumps, fans and compressors are usually modelled as quadratic torque mechanical loads.

In summary, the majority of SPIMs or SASD controlled motors will be mechanically loaded with either constant torque or quadratic torque mechanical load. Besides these two types of mechanical loading, linear torque and constant mechanical power load will also be considered for the completeness of the presented analysis.

3.2 Typical single-phase motors

Single-phase induction motors are often referred to as asymmetrical two-phase induction motors. This is because a motor with a single winding does not develop a rotating magnetic field and therefore can not start on its own. Thus, an auxiliary winding is included, which is shifted 90^o electrically to the main winding, allowing the motor to operate as a two-phase motor during startup.

There are three main types of single-phase induction machines in current use. The simplest type of motor is the “split-phase” or “resistive start - inductive run” (RSIR) motor, Figure 3.1(a). This motor uses the auxiliary winding for start-up, disconnecting it once a certain speed is achieved, and is often used in low starting torque applications. In applications where higher starting torques are required, a capacitor (start capacitor) is placed in series with the auxiliary winding. This motor is referred to as “capacitive start - inductive run” (CSIR), Figure 3.1(b). Where both high starting and high running torques are required, a capacitor (run capacitor) is



(a) RSIR

(b) CSIR

(c) CSR

Figure 3.1: *Three main type of single-phase induction motors.*

permanently connected to the auxiliary winding. This type of motor is referred to as "capacitive start and run" (CSR), Figure 3.1(c). The run capacitor will also improve the power factor of the SPIM, which is poor for RSIR and CSIR motors.

In the analysis presented in this thesis, only steady-state supply and operating conditions are considered, which makes the RSIR and CSIR motors exactly the same. Thus, there are two general variants of motors to be investigated, those that run with a capacitance and those that do not. From the extensive review of manufactures data, it has been found that the majority of lower-power SPIM, typically used in applications such as fridge/freezer and chest freezers, will be either RSIR or CSIR. This is because at lower-power the cost of including a run capacitor is significant when compared to the cost of the motor, outweighing the benefits of improved power factor. Thus, the only case were a run-capacitor may be found in lower-power SPIMs is in applications that require a high running torque. It has also been found, however, that larger motors, mainly used in air conditioners, will tend to be CSR SPIMs.

3.3 Typical single-phase drive applications

Although possible, it is not particularly practical to use a single-phase drive to control a single-phase motor. This is because a standard V/Hz control can not be used to control SPIM speed below 50% of rated speed, [75]. Also, SPIMs are less efficient than three-phase motors rated at the same power. Therefore, the vast majority of SASDs will consist of single-phase

front-end rectifier and a three-phase inverter controlling a three-phase motor, [77]. For that reason, single-phase drives controlling single-phase motors are not considered further in this thesis. The generic circuit of the SASD is shown in Figure 3.2.

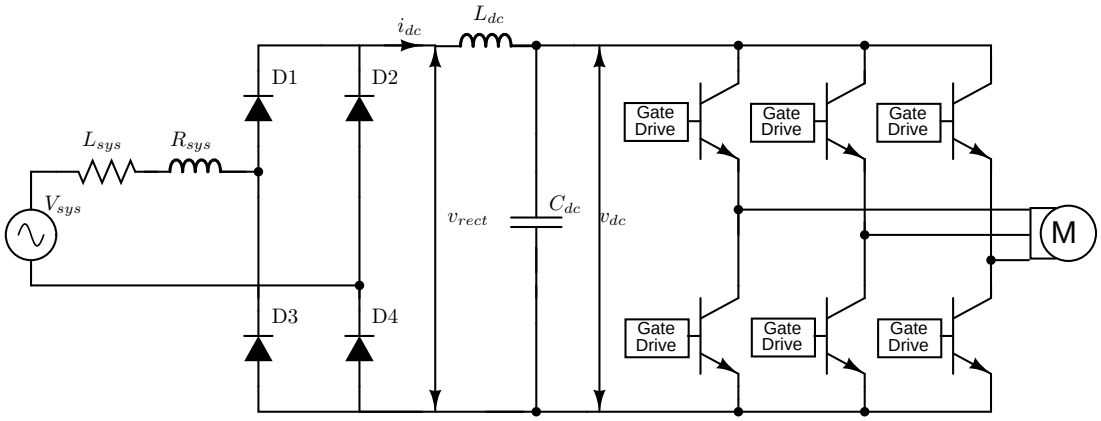


Figure 3.2: *Typical single-phase PWM adjustable speed drive controlling a three-phase motor.*

3.3.1 Rectifier circuit

Similarly to discussed three-phase variant, the passive front-end single-phase diode bridge rectifier is the industry standard circuit for ac to dc voltage conversion. This circuit operates by firstly rectifying the single-phase input ac system voltage, to produce a positive cycle voltage waveform, v_{rect}, at twice the system frequency. This voltage is then applied to the dc link filter, which consists of C_{dc} and L_{dc}. When v_{rect} is greater than v_{dc}, the dc link capacitor will start to charge, drawing current from the supply system, as shown in Figure 3.3. The rate of charge will be influenced by the total resistance and inductance in the charging circuit, as well as the value of C_{dc}. Total resistance is made up of the supply system resistance R_{sys}, any diode forward resistance (likely to be small), the equivalent series resistance of, C_{dc} (likely to be small) and any additional resistance that may be in the rectifier conductance path. It should be noted that in some situations a negative temperature coefficient (NTC) thermistor may be included in the rectifier conductance path. This component has a resistance of $\approx 20\Omega$ when cold and resistance of $\approx 1.5\Omega$ when hot and is used to protect the rectifier components from high inrush currents that can occur on initial connection to the supply system. The total inductance in the circuit will be made up of the local system inductance L_{sys} and L_{dc}, if present.

As the capacitor charges, v_{dc} will increase until it is greater than v_{rect}. At this point, if there was no inductance in the charge circuit, i_{dc} would cease instantaneously. However, as inductance is present in the form of the system impedance and/or L_{dc}, i_{dc} will reduce at a rate determined by this inductance. During the time it takes i_{dc} to reach zero, v_{dc} will continue to increase. Thus, the charging and discharging process results in non-linear operation of the bridge rectifier circuit, as non-sinusoidal current is drawn from the supply system.

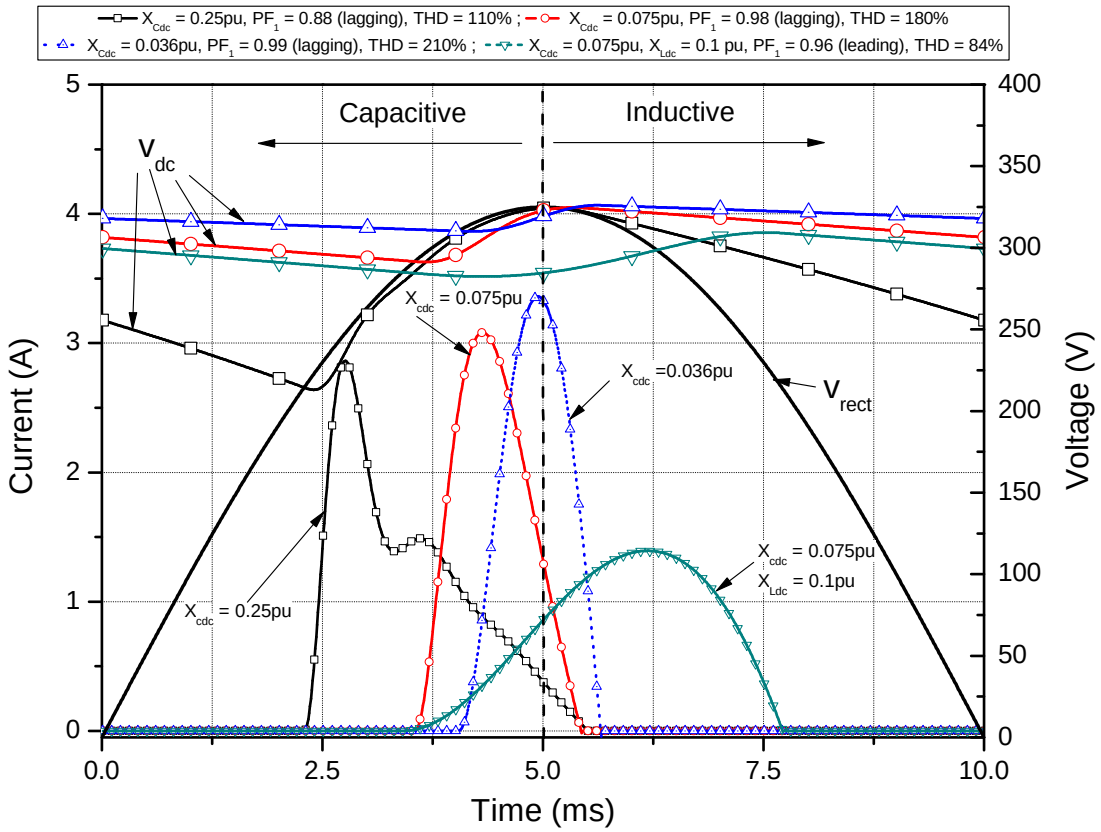


Figure 3.3: *Example waveforms of single-phase rectifier.*

Figure 3.3 shows the effects on the shape of the bridge rectifier input current waveforms of changing the values of dc link filter components C_{dc} and L_{dc}. As can be seen from Figure 3.3, larger values of C_{dc} (corresponding to lower values of $X_{C_{dc}} = \frac{1}{\omega \cdot C_{dc}}$) will lead to narrower and higher peak input current pulses, which are more symmetrical relative to the maximum of the system voltage waveform. This is because larger values of C_{dc} maintain v_{dc} above v_{rect} for longer, and the time for which v_{rect} is greater than v_{dc} is shorter and a narrower current pulse is drawn. Therefore, single-phase rectifiers that have larger values of C_{dc} will draw power from the supply system with close to unity displacement power factor. However, they will draw current with high THD (i.e. high harmonic content) due to the narrow current pulse. It can also be seen in Figure 3.3 that as the value of C_{dc} decreases ($X_{C_{dc}}$ increases) the rectifier input current pulse will shift to the left, causing the rectifier power factor to reduce and the rectifier to operate increasingly as the capacitive load. Conversely, if inductance is added to the bridge rectifier, L_{dc}, the rectifier input current pulse will be shifted to the right, and the rectifier will become an inductive load. It can also be seen that addition of inductance will smooth the rectifier current pulse, as it will decrease both the rate of rise and rate of fall of the input current waveform. Therefore, additional inductance in the bridge rectifier conductance path will reduce harmonic content of the current drawn by the rectifier from the supply system.

3.3.2 Methods of drive-control

The general types of SASDs load will depend on the applied drive control, in the same way as discussed for three-phase ASDs in Section 2.2.2. This is because the inverter in SASDs will be of exactly the same form as the inverter found in ASDs. The vast majority of SASD will be V/Hz PWM type, again because of the simplicity, and therefore low cost, of this type of drive control. However, some specific SASD applications may use more advanced vector control. For example, [73] states that the next generation of washing machines will use space vector controlled SASDs. Accordingly, both V/Hz and vector controlled drives are considered in the analysis presented in this chapter.

3.4 Modelling of single-phase directly connected and drive-controlled motors

This section introduces the SPIM and SASD drive models analysed in this chapter. PSpice software was once again employed, due to its non-linear semiconductor modelling capabilities. The developed PSpice models also provide verification of the MatLab/SimuLink in-built SPIM model, as there was a lack of measurement data.

3.4.1 Motor modelling

The standard dq model was selected to represent the SPIM in this analysis. This model is derived in a similar way to that of the dq model of the three-phase induction machine. This dq SPIM model is described by (3.1), with the corresponding equivalent circuit shown in Figure 3.4. Full details on the derivation of this model can be found in [50].

$$\begin{bmatrix} v_{qs}^{s} \\ v_{ds}^{s} \\ v_{qr}^{'s} \\ v_{dr}^{'s} \end{bmatrix} = \begin{bmatrix} r_s + \rho L_{ss} & 0 & \rho L_{ms} & 0 \\ 0 & r_S + \rho L_{SS}\rho & 0 & \rho L_{mS} \\ \rho L_m s & -\frac{\omega_r}{n} L_{mS} & r_r^{'} + \rho L_{rr}^{'} & -\frac{\omega_r}{n} L_{RR}^{'} \\ n\omega_r L_{ms} & \rho L_{mS} & n\omega_r L_{rr}^{'} & r_R^{'} + \rho L_{RR}^{'} \end{bmatrix} = \begin{bmatrix} i_{qs}^{s} \\ i_{ds}^{s} \\ i_{qr}^{'s} \\ i_{dr}^{'s} \end{bmatrix} \tag{3.1}$$

where: $L_{ss} = L_{ls} + L_{ms}$
$L_{SS} = L_{lS} + L_{mS}$
$L_{rr}^{'} = L_{lr}^{'} + L_{ms}$
$L_{RR}^{'} = L_{lR}^{'} + L_{mS}$
$n = \frac{N_S}{N_s}$.
and: L_{ls}, r_s, $r_r^{'}$, $L_{lr}^{'}$ are the main winding stator and rotor inductances and resistances and L_{lS},

r_S, $r_R^{'}$, $L_{lR}^{'}$ are the auxiliary winding stator and rotor inductances and resistances.

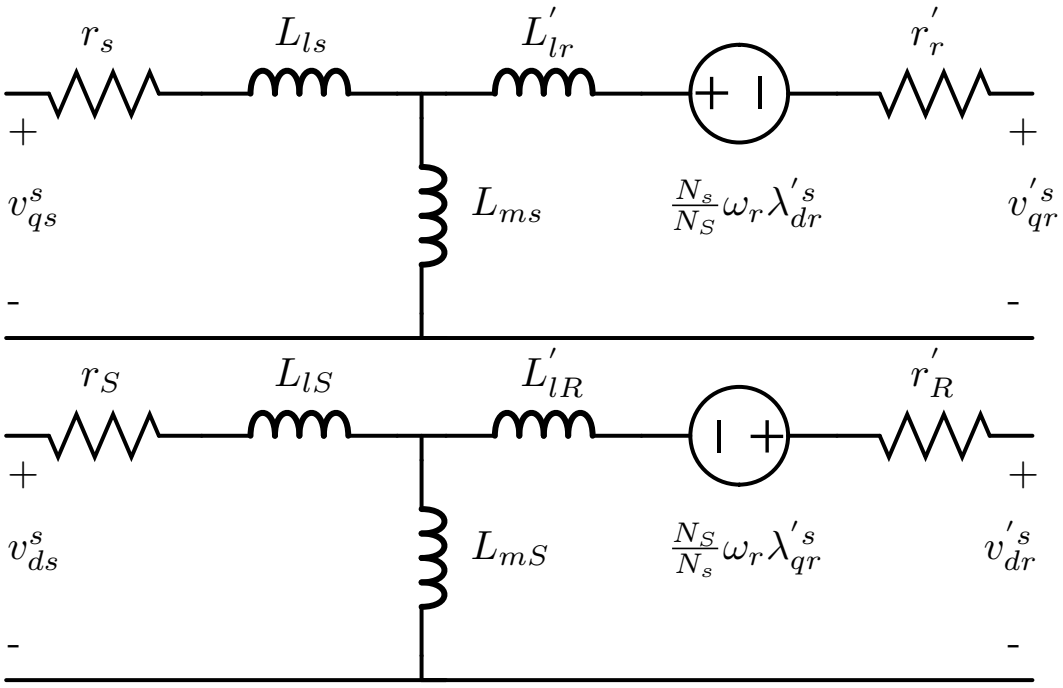


Figure 3.4: *Stationary reference dq single-phase induction motor circuit representation.*

3.4.2 Development of PSpice single-phase induction motor models

The presented dq SPIM model was implemented directly in PSpice, with circuit schematic shown in Appendix B.1. In order to validate implemented PSpice SPIM model, results of simulations were compared with those produced by the in-built SimuLink SPIM model, [53]. A $\frac{1}{4}$ hp (180W) SPIM, with parameters taken from [50], was used for the comparison of the two models. Figure 3.5 shows the results of this comparison, where both motor models are energised and allowed to reach full rated speed unloaded, and then loaded with rated mechanical load. The comparison shows that the PSpice and SimuLink models match each other well, with respect to steady-state rotor speed, steady-state rotor mechanical torque and steady-state stator input current. There are differences in the transient characteristics of the two motor models, which are the result of each model having different values of machine inertia. The standard machine inertia values were not matched, as this analysis is only concerned with steady-state operation.

3.4.3 Development of PSpice single-phase drive controlled motors

The three-phase inverter used in the SASD is of exactly the same form as the inverter developed and validated in Section 2.3.3. Therefore, this validation is not repeated here. The PSpice schematic of the SASD can be found in Appendix B.1.

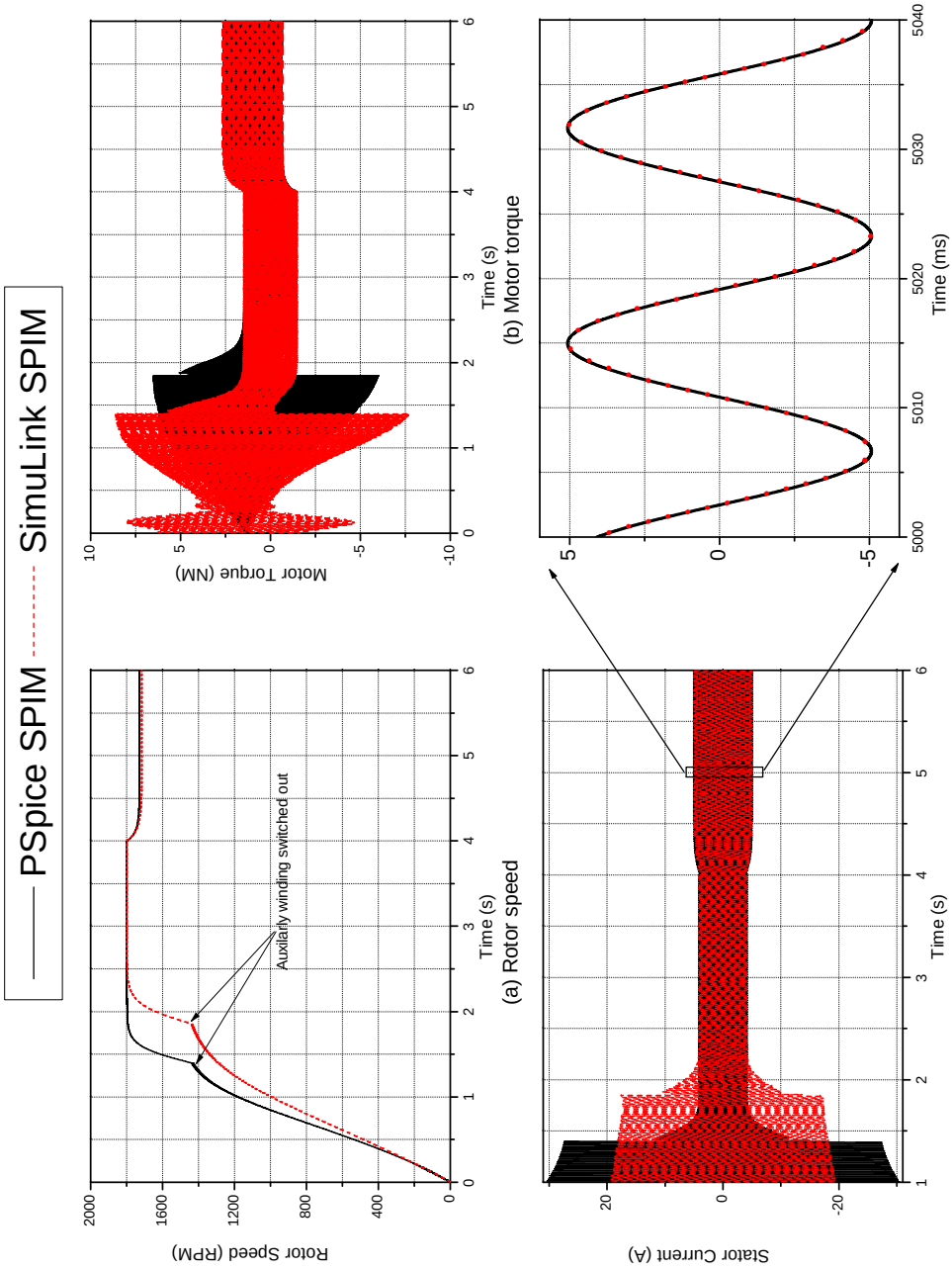


Figure 3.5: *Comparison between PSpice and SimuLink results for resistive start - inductive run (RSIR) single-phase induction motor.*

3.5 Typical values of dc link filter components

As SASD are a relatively new type of load, there is a lack of literature about typical values of dc link filter components, L_{dc} and C_{dc}. In order to predict the most likely values of these components, three-phase ASDs are taken as a reference point, as the difference between SASD and ASD is merely in the 'front-end' bridge rectifier. In the case of ASDs, the value of C_{dc} is typically selected such that the dc link voltage ripple will be in the range of 5% to 20%, where larger capacitor values result in lower ripple.

The SASD model developed in the previous section was used to investigate the values of C_{dc} that would give 5% to 20% ripple in the SASD dc link voltage. It was found that the per unit values of $X_{C_{dc}}$ in the SASD were close to 0.0015 - 0.12 with 0.075 nominal, i.e. approximately three times the size of C_{dc} that would be used in an ASD of the same rated power (see Section 2.4). This is because the ASD dc link will be charged by the rectified system voltage six times per fundamental period, compared to two times in the case of the SASD. Thus, for the same rated power and value of C_{dc}, the SASD will exhibit three times as large dc link ripple. Accordingly, the value of C_{dc} in the SASD should be three times bigger than in the ASD, to give the same voltage ripple. The expected per-unit value of C_{dc} in SASD may therefore be found in the same way as for the ASD, i.e. using expressions (2.4) and (2.5).

The value of L_{dc}, however, will be very much dependent on harmonic legislation, which is discussed in the following section.

3.6 Harmonics limits

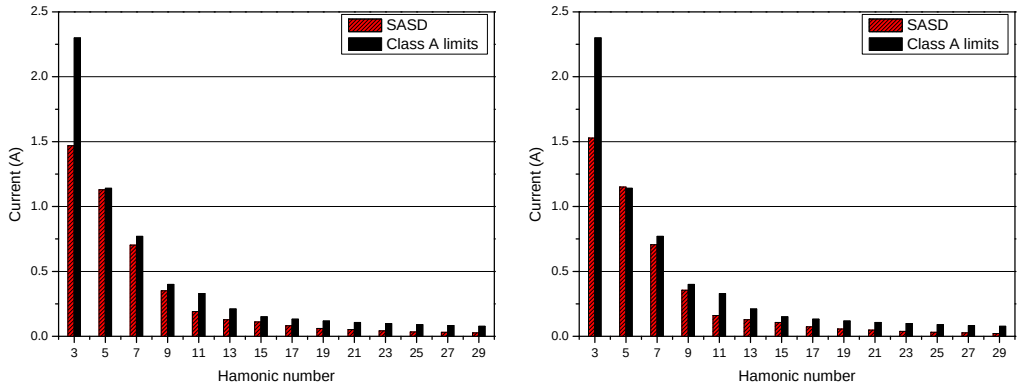
Single-phase adjustable speed drives, due to the non-linear operation of the front-end single-phase bridge rectifier, will draw non-sinusoidal current from the supply system, rich in harmonics. If these loads are to be connected to the EU supply systems, they must conform to harmonic limits stipulated in [30]. The vast majority of the SASDs will be of rated power less than 1 kW, and Class A harmonic limits from [30] will apply. Class A limits are summarised in Table 3.3.

To investigate the harmonic content of the SASD input current waveform, and its relation to Class A harmonic limits, the full PSpice model of the SASD is used. The SASD model was run at different rated powers by altering the mechanical loading on the SASD. At each rated power, the absolute value of C_{dc} was adjusted so as to maintain nominal per-unit value as given in Section 3.5. For this analysis, L_{dc} was set to zero. The harmonic content of the SASD input current waveform was compared to Class A limits at each rated power. It was found that SASD with rated active power less than 390W, could meet the Class A harmonic limits, while

Table 3.3: *Harmonic limits for Class A load, [30].*

Harmonic order n	Max. harmonic current (A)
Odd harmonics	
3	2.3
5	1.14
7	0.77
9	0.40
11	0.33
13	0.21
$15 \leq n \leq 39$	$0.15\frac{15}{n}$
Even harmonics	
2	1.08
4	0.43
6	0.30
$8 \leq n \leq 40$	$0.23\frac{8}{n}$

SASD with higher rated power could not. Figure 3.6 shows the SASD input current harmonics for 380W and 400W SASDs compared to Class A limits. It can be seen from this figure that at 400W the 5^{th} harmonic of the SASD input current just breaches the Class A limits. Thus, at rated power above approximately 390W SASDs will require some form of power factor correction (PFC) in order to comply with Class A harmonic limits. There are two general types of PFC, passive PFC and active PFC, each of which are now discussed.



(a) Rated power = 380W (b) Rated power = 400W

Figure 3.6: *Harmonic content of SASD input current at different rated power compared with Class A harmonic limits.*

3.6.1 Passive power factor correction

Passive power factor correction is implemented by introducing and setting the value of dc link filter inductor L_{dc} (see Figure 3.2) so that necessary harmonic limits are achieved. Additional inductance in the SASD's bridge rectifier will widen the current pulse drawn by the rectifier, and therefore reduce its harmonic content, as discussed in Section 3.3.1 and shown in Figure 3.3.

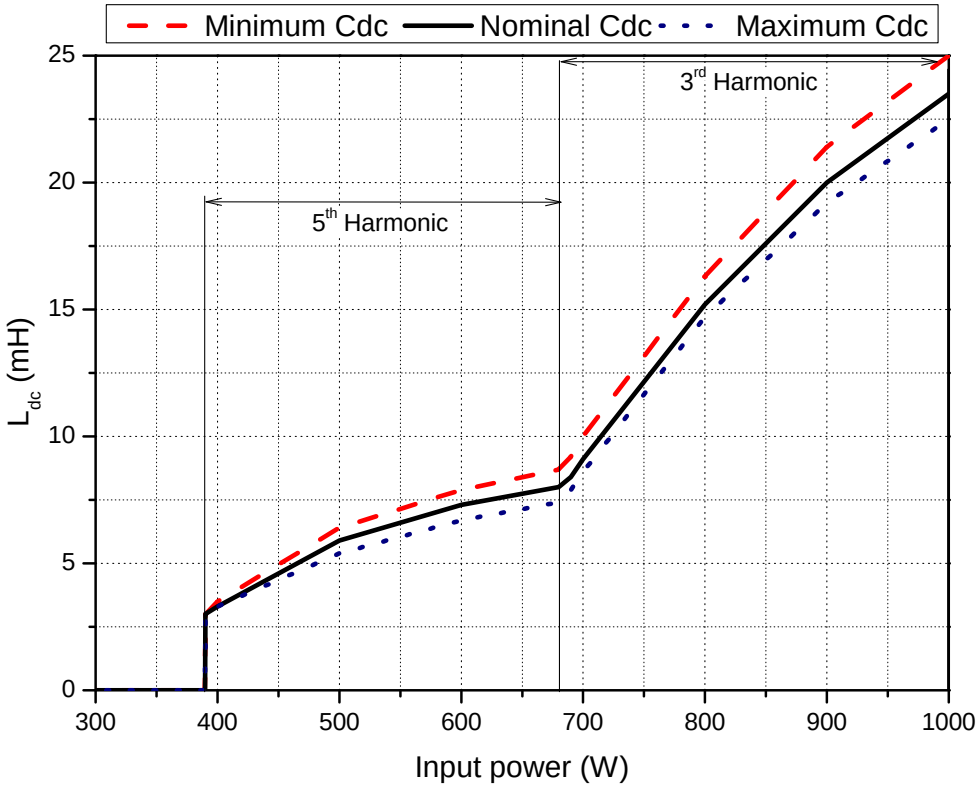


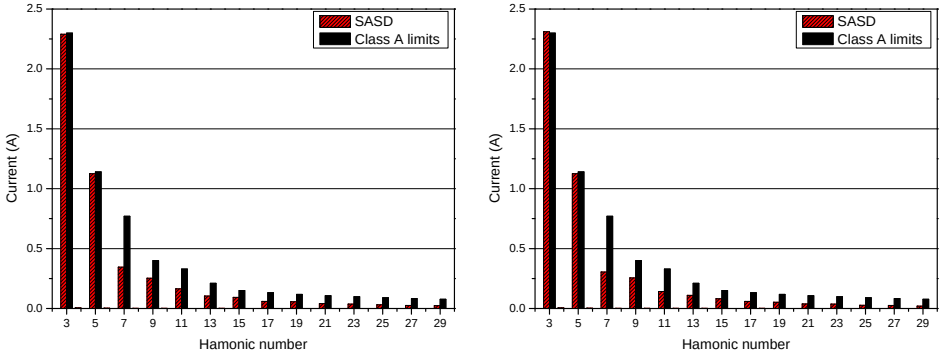
Figure 3.7: *Minimum size of L_{dc} to meet Class A harmonic limits for SASD at different rated powers and range of values of C_{dc}.*

Simulations were again run using the full PSpice SASD model in order to find minimum required value of L_{dc} to meet Class A harmonic limits. The analysis was performed for SASD of different rated power from 380W-1kW. The values of C_{dc} in each SASD were taken as minimum (0.0015pu), nominal (0.075pu) and maximum (0.12pu), as presented in Section 3.5, so that likely variation in the value of C_{dc} is also considered in the analysis. Figure 3.7 shows these results.

The results presented in Figure 3.7 show two distinctive regions in the L_{dc} versus P_{rated} characteristics of the SASD load type. The shape of this characteristic is due to Class A harmonic limits being specified as current magnitudes, which are independent of the rated power of the SASD. In the section of Figure 3.7 labelled '5^{th} harmonic', the limit for this harmonic will be dictating the value of L_{dc}, as the rated power of the SASD is still too low to cause the 3^{rd} harmonic to breach specified limits. In the section labelled '3^{rd} harmonic', the Class A limit for the 3_{rd} harmonic will dictate the value of L_{dc}.

Figure 3.8(a) shows the harmonic content of the SASD's input current for SASD rated at 680W and value of L_{dc} selected so the 5^{th} harmonic is just met. It can be seen from this figure that the 3^{rd} harmonic is not being breached. If the power of the SASD is increased to 700W and the value of L_{dc} is again adjusted to meet 5^{th} harmonic limits, Figure 3.8(b) is obtained. This figure shows that although the 5^{th} harmonic limit is met, the 3^{rd} harmonic will not be, and from this

power onwards the value of L_{dc} must be selected to meet the 3^{rd} harmonic. Figure 3.7 shows that larger values of C_{dc} are required per watt of SASD to meet the 3^{rd} harmonic as opposed to the 5^{th}, hence difference in gradients shown in this figure.



(a) Rated power = 680W (b) Rated power = 700W

Figure 3.8: *Harmonic content of SASD input current at different rated power compared with Class A harmonic limits.*

It can be further seen from Figure 3.7 that the considered range of values of C_{dc} will have only a small effect on the value of L_{dc}. This is because the value of L_{dc} will have dominant influence on the harmonic content of the SASD input current.

3.6.1.1 Active power factor correction

An alternative to passive PFC is active PFC. Active PFC operates on the principle of current shaping, using a dc-dc converter, typically based on standard boost-converter topology, Figure 3.9. The current flowing through the inductor L_{a1} is controlled and shaped to be a good approximation of the input system voltage waveform. Active PFC also has the advantage of providing ac line regulation, keeping the dc link voltage effectively constant with the changes in supply system voltage. Currently, active PFC is less common than passive PFC, due to the higher costs and increased losses associated with the extra switching stage in the drive circuit.

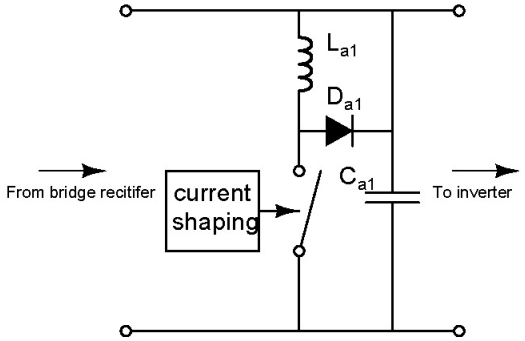


Figure 3.9: *Typical active power factor correction topology.*

3.7 Active and reactive power demand characteristics of single-phase directly connected induction motors

This section investigates the characteristics of two general types of SPIM (those with a run capacitor and those without). The motor model used for this investigation was a 180W SPIM, with motor parameters taken from [50]. This motor was implemented in both PSpice and MatLab using the dq model presented previously in this chapter. Simulations were then run to obtain the active and reactive power demand characteristics with change in system voltage and change in motor mechanical loading condition for both RSIR and RSCR SPIMs. Figures 3.10 and 3.11 show the results of this analysis for each type of SPIM. The results for P-V and Q-V characteristics are presented as per-unit values, where active and reactive power bases are the nominal active and reactive power of the RSIR SPIM (i.e. RSIR SPIM run at nominal speed with nominal voltage applied and nominal mechanical loading conditions).

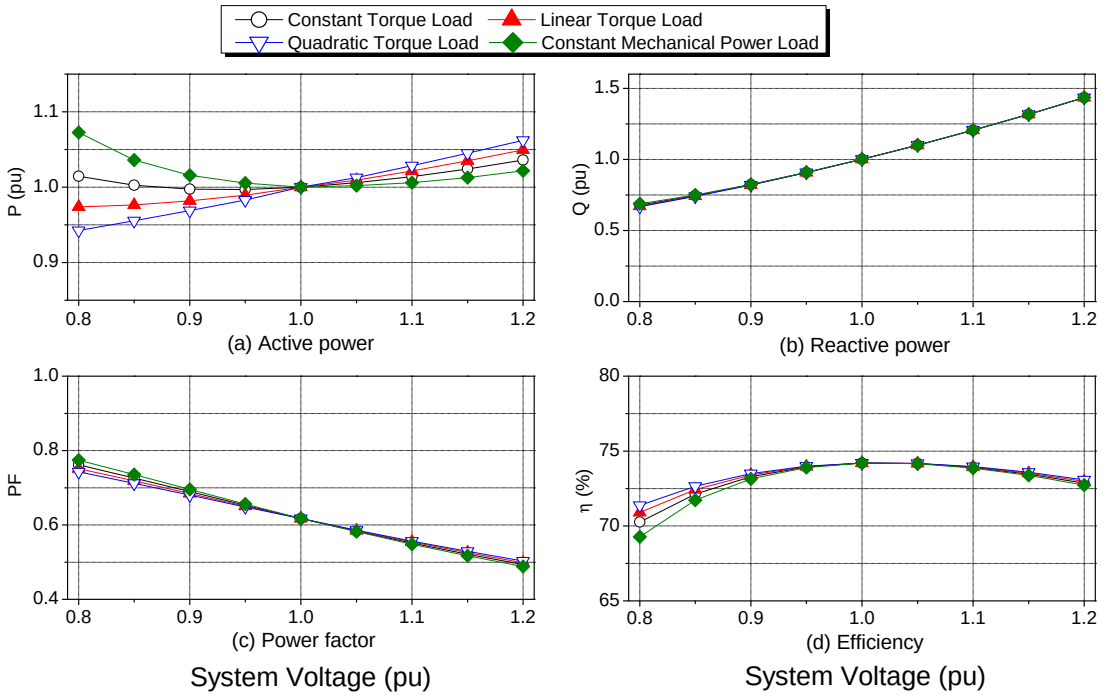


Figure 3.10: *Characteristics of directly connected 180W RSIR SPIM for four different types of mechanical loading.*

Figure 3.10 shows that the P-V characteristics of the RSIR SPIM are influenced by the type of mechanical loading applied to the motor. A maximum difference of 10%, at 0.8pu system voltage, in active power demand can be seen between the RSIR SPIM mechanically loaded with quadratic torque and constant mechanical power loads. At higher values of system voltage, this difference decreases to 5% at 1.2pu system voltage. The $\eta - V$ characteristics of the RSIR SPIM decreases as the motor is operated at other than nominal values of system voltage. The nominal efficiency of this motor is 74%, which, although low, is common for this size and type of motor. The main reason for poor efficiency is that the RSIR SPIM operates at low power factor which

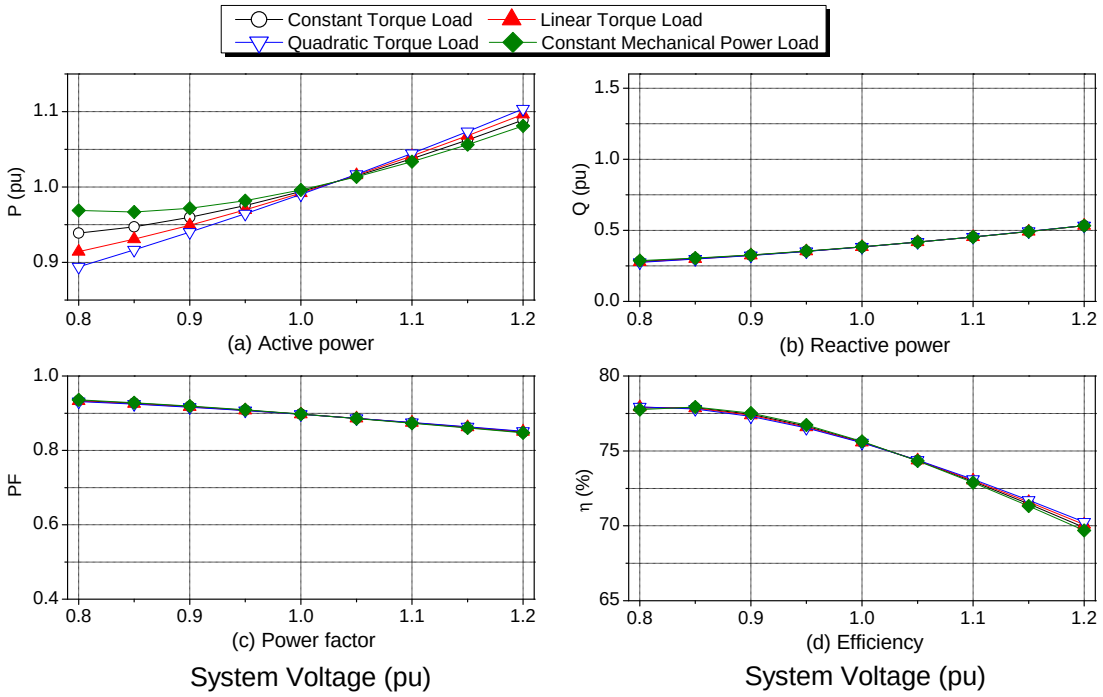


Figure 3.11: *Characteristics of directly connected 180W RSCR SPIM, for four different types of mechanical loading.*

is about, 0.6 at nominal voltage. Similarly to directly connected three-phase motors, the power factor of the RSIR SPIM will improve with reduced system voltage, and worsen with increased system voltage. The mechanical loading on the RSIR SPIM will also have little effect on its power factor. These PF-V characteristics are due to the motor magnetisation branch, which dictates reactive power consumption of the SPIM, while the stator and rotor inductances have much lower influence on these characteristics. Accordingly, the Q-V characteristics of the RSIR SPIM will be essentially independent of types of mechanical loading, as can be seen in Figure 3.10(b).

Figure 3.11 shows that the inclusion of a run capacitor in the SPIM has a significant effect on motor characteristics. Firstly, the RSCR motor's P-V characteristics are more linear, and the effect of different applied mechanical load on P-V characteristics is reduced compared to the RSIR SPIM. The maximum difference between P-V characteristics can again be found between the RSCR SPIM mechanically loaded with quadratic and constant mechanical power loads, but this time the difference is about 5% at 0.8pu system voltage and 2% at 1.2pu system voltage. The RSCR SPIM P-V characteristics differ from the RSIR SPIM's because the run capacitor changes the $\eta - V$ characteristics of the RSCR SPIM. This is because the run capacitor improves the motor power factor to a nominal value of 0.9, also improving the efficiency of the RSCR SPIM. The power factor again increases with the reduction in system voltage and reduces with increased system voltage. However, the variation in these PF-V characteristics is much less

than those of the RSIR SPIM. Therefore, the RSCR SPIM will draw considerably less reactive power than the RSIR SPIM. As in the case of RSIR SPIM, the effect of motor mechanical loading condition on RSCR SPIM Q-V characteristics is negligible.

3.8 Exponential and polynomial load models of directly connected single-phase induction motors

From the analysis of SPIM active and reactive power characteristics in the previous section, it was shown that the P-V characteristics of these motors will depend on the type of applied mechanical load and the type of SPIM (RSIR or RSCR). Thus, separate exponential and polynomial models for their P-V characteristics should be implemented for each type of considered mechanical loading condition and each type of SPIM. However, the Q-V characteristics of SPIMs are not significantly affected by the type of mechanical loading, only by the type of SPIM. Accordingly, common exponential and polynomial models may be used to represent the Q-V characteristics of the same type of SPIM with different mechanical loading conditions. Exponential and polynomial models were fit using the least square method method described in Section 2.7.1, to the results presented in Figures 3.10 and 3.11. The resulting exponential and polynomial model coefficients are presented in Table 3.4. Figures 3.12 to 3.14 show these exponential and polynomial models compared to the full model, illustrating their ability to represent the required P-V or Q-V characteristics. Additionally, previously presented load model of SPIMs from literature (Table 3.2), are also shown in Figures 3.12 to 3.14.

Table 3.4: *Proposed exponential and polynomial model coefficients of single-phase induction motors.*

Loading	PF_{nom}	Exp. Model		Polynomial Model					
		np	nq	Z_p	I_p	P_p	Z_q	I_q	P_q
RSIR CT	0.62	0.06	1.92	0.63	-1.20	1.57	1.40	-0.91	0.50
RSIR LT	0.62	0.19	1.92	0.31	-0.43	1.11	1.40	-0.91	0.50
RSIR QT	0.62	0.30	1.92	0.10	0.10	0.80	1.40	-0.91	0.50
RSIR CP	0.62	-0.12	1.92	1.16	-2.42	2.26	1.40	-0.91	0.50
RSCR CT	0.90	0.38	1.68	0.50	-0.62	1.11	1.54	-1.43	0.89
RSCR LT	0.90	0.46	1.68	0.34	-0.22	0.88	1.54	-1.43	0.89
RSCR QT	0.90	0.53	1.68	0.22	0.08	0.69	1.54	-1.43	0.89
RSCR CP	0.90	0.29	1.68	0.73	-1.16	1.43	1.54	-1.43	0.89

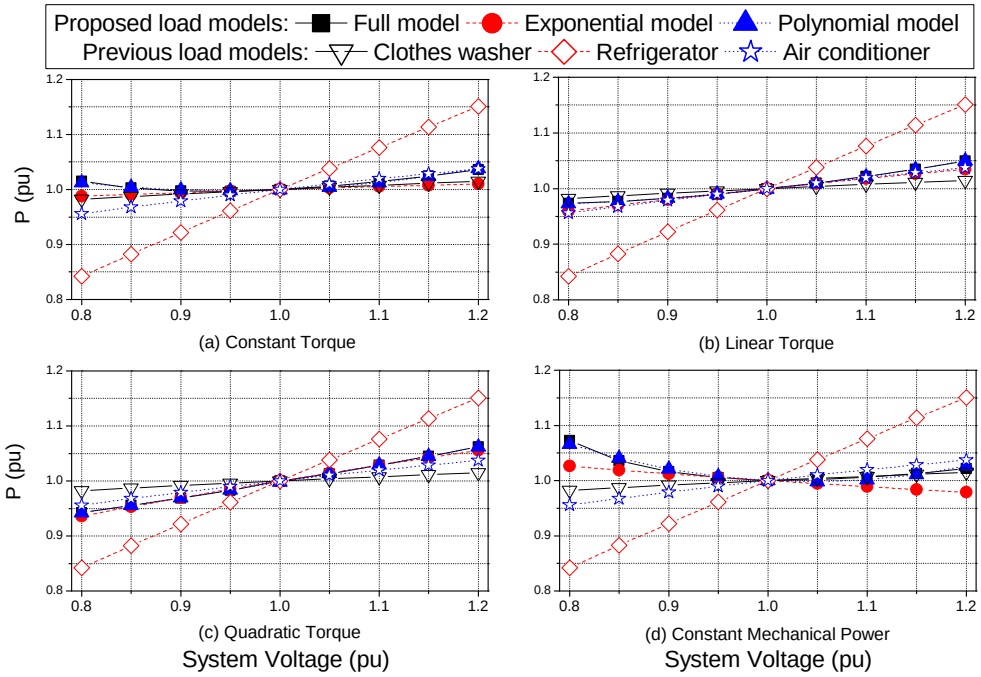


Figure 3.12: *Exponential and polynomial model fits for RSIR SPIM active power characteristics.*

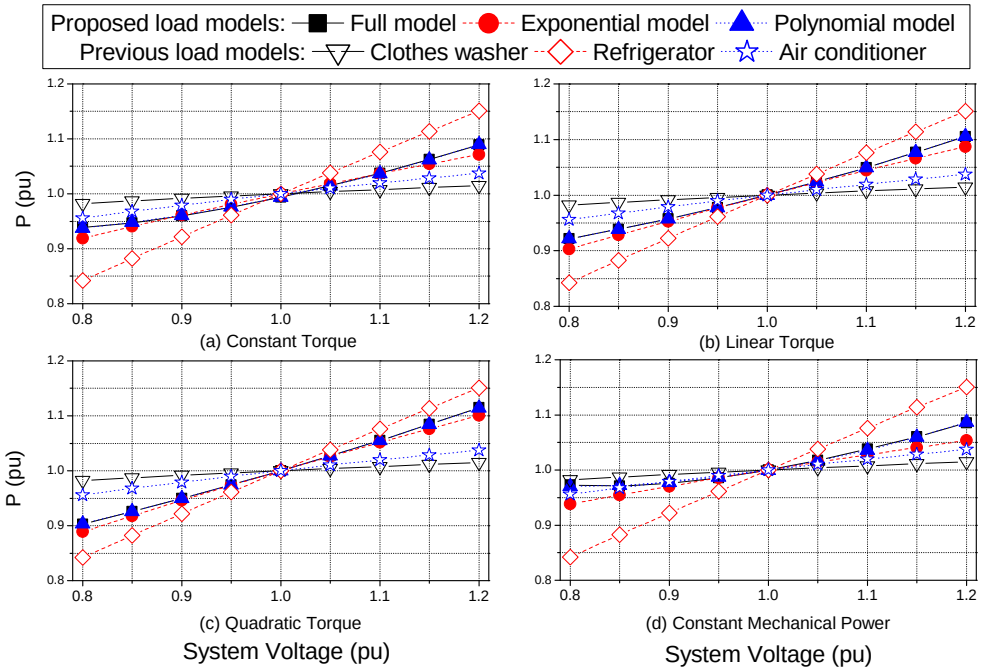


Figure 3.13: *Exponential and polynomial model fits for RSCR SPIM active power characteristics.*

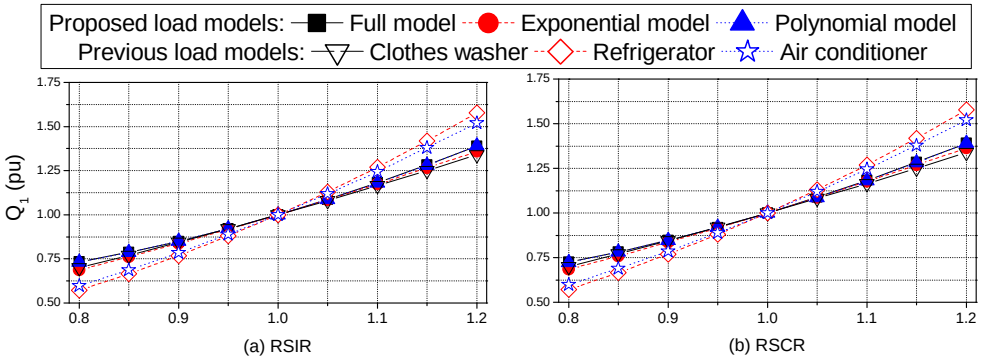


Figure 3.14: *Exponential and polynomial model fits for RSIR and RSCR SPIMs reactive power characteristics.*

It can be seen from Figures 3.12 to 3.14 that the polynomial model can fit the required characteristics with no significant error. However, the exponential model does show (small) error for all fits. This error is greater for the less linear motor characteristic, which is expected and due to the simplicity of the exponential model.

It can be seen from Figure 3.12 that the P-V and Q-V characteristics of the previously presented clothes washer load model (Table 3.2) match almost perfectly to those of the RSIR SPIM with constant mechanical torque load. This makes sense, as from discussions in Section 3.1.1 washing machines are expected to have constant torque mechanical loading. The power factors of these two load models are also in good agreement. The previously presented load models of air conditioner load have also very similar P-V characteristics to RSIR SPIM, but this time with quadratic torque load, again in agreement from discussion in Section 3.1.1. The Q-V characteristics of these two load models are also similar, but the power factors are different. It should be noted that the power factor of the previously presented air conditioner load model is 0.96, which seems unusual for a single-phase motor. However, no further comment about this previously presented load model is made, and no further information was provided in [15] as to what type of motor was considered. Finally, the P-V and Q-V characteristics of previously presented refrigerator load model most closely match those of the proposed RSCR SPIM, Figure 3.13, with quadratic torque load. The power factors of the proposed model is higher than that of the previous model of refrigerator. Again, no further information was provided in [15] about the measured refrigerator, other than it was measured in 1979.

From these comparisons, general agreement can be seen between P-V and Q-V characteristics of previously developed load models of single-phase induction motors and those proposed in this thesis. Power factors of all but one of the previously presented load (washing machine load) are, however, in disagreement.

3.9 Active and non-active power demand characteristics of SASDs

The voltage source inverter (VSI) drive, introduced in Section 3.3, was applied to a 736W (1hp) three-phase induction motor (with parameters found in [78]), to form the general SASD model. Four different types of SASDs are investigated: V/Hz open-loop, V/Hz closed-loop, direct torque controlled (DTC) and SASD with active power factor correction. V/Hz controlled open-loop SASDs are expected to be the most common type of SASD at present, although the number of SASD with advanced control (DTC) are expected to increase in the near future. Field oriented control (FOC) drives are not specifically analysed, as it was shown in Section 2.8 that active and non-active power characteristics of DTC and FOC SASDs are essentially the same.

Following a similar procedure to that described in Section 2.8, active and non-active power demand characteristics of considered SASDs mechanically loaded with four general mechanical load types are analysed. Nominal values of dc link filter components are selected, i.e. the per-unit value of $X_{C_{dc}}$ is taken as 0.075 (Section 3.5) and the value of L_{dc} is selected based on the results presented in Figure 3.7. The results of this analysis are presented in per-unit. Again, the base for the per-unit active and reactive powers were taken as the nominal active and fundamental reactive power demand of the considered SASDs. The one exception is SASD with active power factor correction, for which the base fundamental reactive power is taken as that of the V/Hz open-loop SASD. As the SASDs to be investigated are all of similar rated active power, a common system impedance was taken. The value of the system impedance is selected as the nominal value used in this thesis. (see Section 1.8).

3.9.1 V/Hz open-loop controlled SASDs

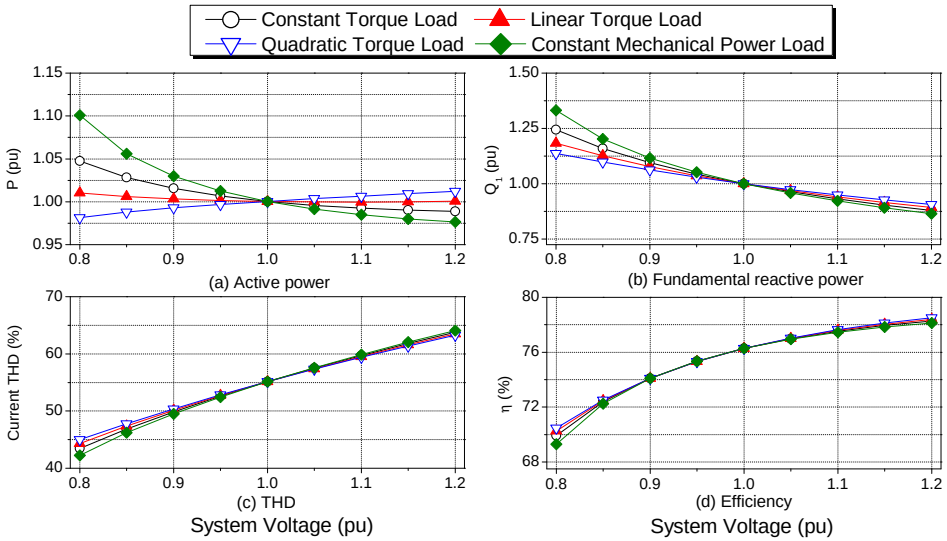


Figure 3.15: *Characteristics of 736W open-loop V/Hz controlled SASD for four different types of mechanical loading.*

3.9.2 V/Hz closed-loop controlled SASDs

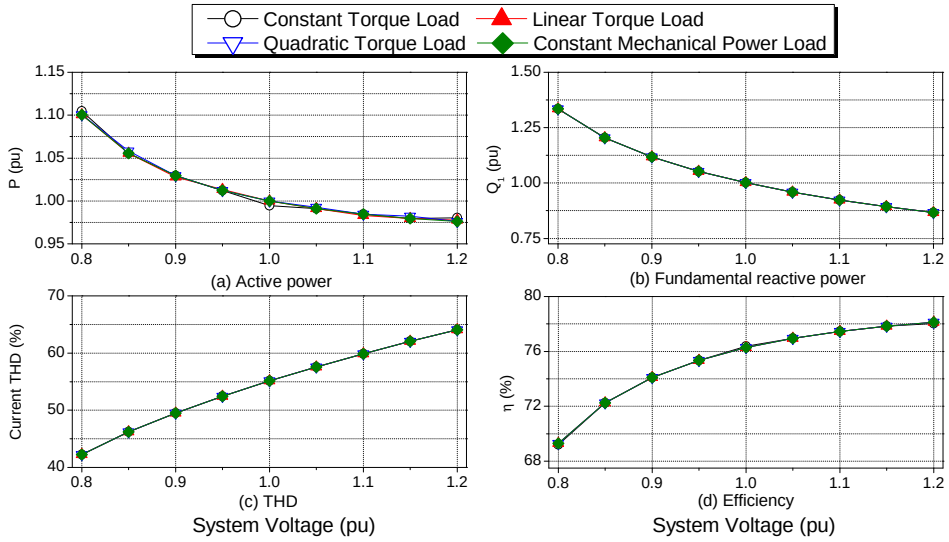


Figure 3.16: *Characteristics of 736W closed-loop V/Hz controlled SASD for four different types of mechanical loading.*

3.9.3 SASDs with advanced control

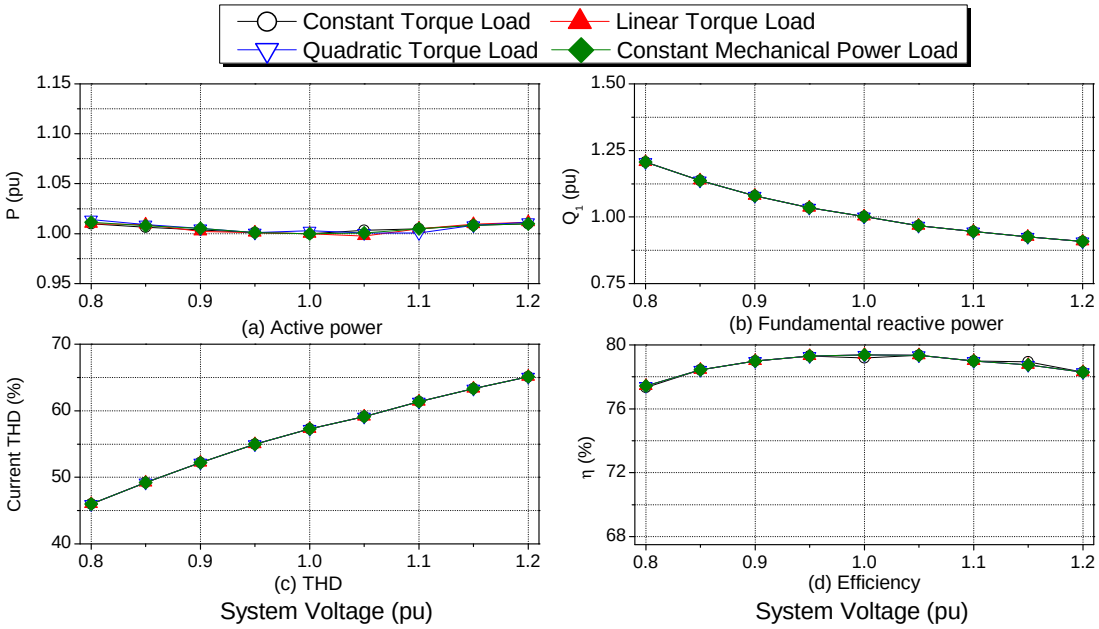


Figure 3.17: *Characteristics of 736W direct torque controlled SASD for four different types of mechanical loading.*

3.9.4 SASD with active power factor correction

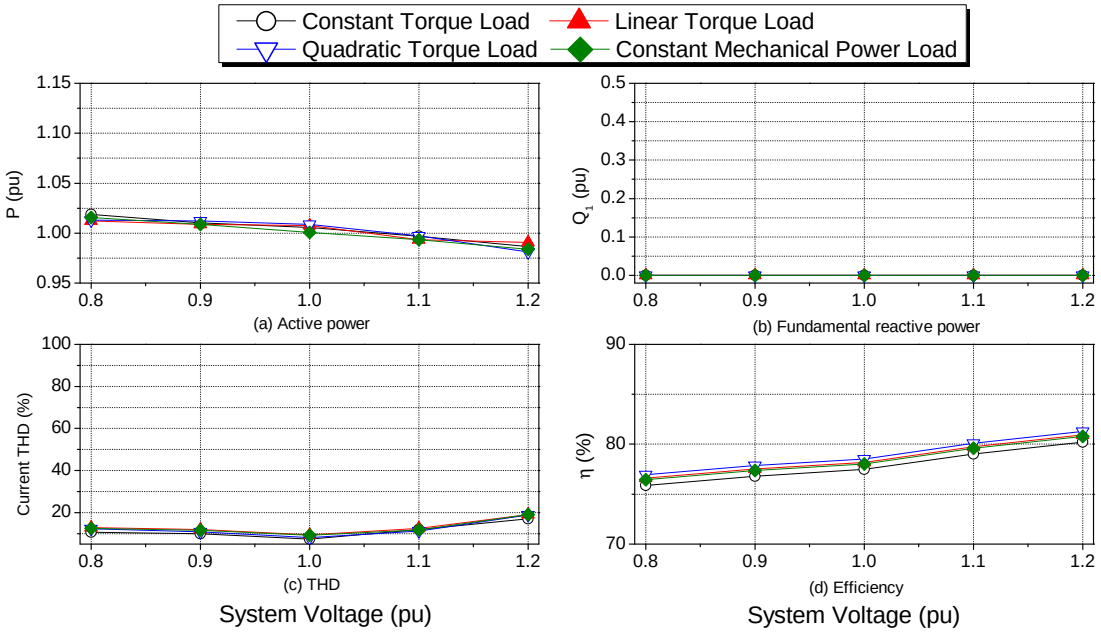


Figure 3.18: *Characteristics of 736W open-loop V/Hz controlled SASD with active power factor correction for four different types of mechanical loading.*

3.9.5 Discussion of active and non-active power demand characteristics

The P-V characteristics of the V/HZ open-loop, closed-loop and advanced control SASDs, shown in Figures 3.15(a), 3.16(a) and 3.17(a), are almost identical to those of the corresponding 4kW ASDs, previously presented in Section 2.8.2. This shows that the type of drive front-end (single-phase or three-phase), will have little effect on active power demand characteristics, as the motor will dictate these characteristics. This result also further extends the considered range for lower-power three-phase motors, showing that the 4kW three-phase motor is indeed representative of the characteristics of sub-kW rated three-phase motors. The efficiency of the 736W SASD is lower than that of the 4kW ASD, as would be expected. The shape of these P-V and $\eta - V$ characteristics are not considered further here, as they have already been discussed in Section 2.8.2 for 4KW ASDs, and exactly the same principles apply for SASDs.

The non-active power demand characteristics of the SASDs, shown in Figures 3.15(b) and (c), 3.16(b) and (c) and 3.17(b) and (c), do not match those of the 4kW ASDs, although they are also independent of the type of drive control. In the same way for the ASD load, the non-active power characteristics of the SASD will be dominated by the front-end bridge rectifier. The majority of the remainder of this chapter is dedicated to quantifying and representing these characteristics, and further discussion is deferred until more data has been presented.

The results presented in Figure 3.18 show the changes in active and non-active power demand

characteristics of SASD with added active PFC circuit. The active PFC circuit is effectively keeping the dc link voltage constant over the considered range of supply system voltages, which influences that the speed of the motor (and mechanical power at the shaft of the machine) will remain constant. The slight increase in input active power at the lower values of the system input voltage is due to the increased current drawn by the active PFC circuit, causing increased losses. Accordingly, the active PFC circuit will reduce the overall efficiency of the SASD, when compared to the efficiency of the drives without the active PFC circuit. The fundamental reactive power drawn from the supply system is essentially zero, for the considered voltage range, as the active PFC circuit corrects the displacement PF to near unity. The total harmonic distortion of the input current waveform is also near zero, but increases slightly at higher voltages. This is because toward 1.2pu system voltage the modelled active PFC correction circuit is approaching its maximum rated voltage, and is not able to maintain a low current THD value.

3.9.6 Summary of presented SASD characteristics

From the results presented so far in this chapter, it has been shown that the P-V characteristics of SASDs may be represented in exactly the same way as those of lower-power ASDs presented in Section 2.8. This is because the P-V characteristics of V/Hz controlled SASDs are dictated by the controlled three-phase motor, which is common to both ASDs and SASDs. Similarly, the P-V characteristics of SASDs with advanced control are determined by the applied control strategy, which is also the case with ASDs.

The active power demand characteristics of SASDs with active power factor correction circuits have been shown to be essentially constant for the considered changes in system voltage, while their Q_1-V and THD-V characteristics are close to zero. Thus, SASDs incorporating active power factor correction techniques may be assumed to be constant (active) power loads operating at unity power factor for the purposes of steady state load representation.

The non-active power demand characteristics of V/Hz and advance controlled SASDs have been shown to be similar. However, it is known from the results presented in the previous chapter for ASDs that these N-V characteristics will depend on the values of dc link filter components in the SASD bridge rectifier, the mechanical loading on the SASD and to a certain extent system impedance. These N-V characteristics are further investigated in the next sections, where an analytical model of SASDs is also developed in order to represent their characteristics without the use of a full SASD model.

3.10 Analytical model of SASDs

It has been shown in the preceding sections that SASDs have almost exactly the same active power demand characteristics as ASDs. This is because the only difference between SASD and ASD is the font-end bridge rectifier, while the inverter and motor are common to both loads. Therefore, exactly the same equivalent resistance model for the representation of the inverter and motor, developed for ASDs in Section 2.10, is used for the representation of inverter and motor in SASDs. The equivalent circuit model of the SASD is shown in Figure 3.19. The equivalent resistance in Figure 3.19 is represented by (2.11) to (2.14) for different types of motor mechanical load.

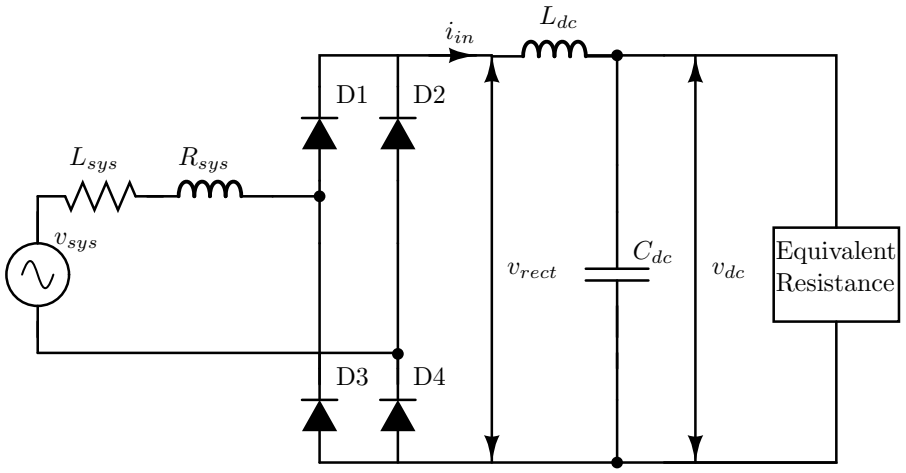


Figure 3.19: *Equivalent circuit model of SASD.*

In order to convert the equivalent circuit model of the SASD into analytical form, an analytical model of the single-phase bridge rectifier must be developed first.

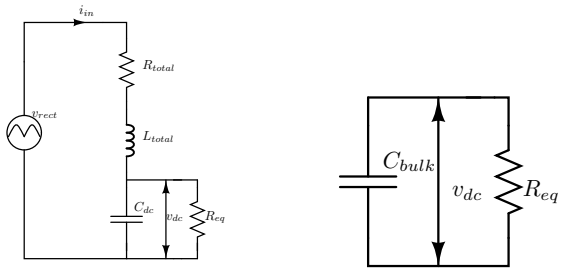
3.10.1 Analytical representation of single-phase bridge rectifier

As previously discussed in Section 3.3, the single-phase diode bridge rectifier has two distinctive periods of operation, defined by the charging or discharging state of the link capacitor, C_{dc}. The charging state may be represented by a RLC circuit driven by the rectified system voltage, v_{rect}. The diagram of this equivalent charging circuits is shown in Figure 3.20(a).

The total resistance of the charging circuit, R_{total}, represents the sum of all resistances in the bridge rectifier charging conduction path, i.e. the local supply system resistance, the resistance of NTC thermistor if present, the resistance of the bridge diode, the equivalent series resistances of the dc link capacitor and inductor (if present) and the resistance of any circuit connections in the rectifier conduction path. In a similar way, the total inductance, L_{total}, represents the sum of

the supply system inductance and dc link filter inductance (if present). The circuit capacitance is directly represented by the dc link capacitor, C_{dc}. The discharging operating state of the bridge rectifier is represented by the circuit shown in Figure 3.20(b). This circuit is a simple RC discharge circuit, where value of the equivalent resistance and size of C_{dc} dictate the rate of discharge of capacitor voltage, v_{dc}.

These charge and discharge circuits may be represented analytically by the differential equations (3.2) and (3.4).



(a) Charging Circuit (b) Discharging Circuit

Figure 3.20: *Equivalent circuit representation of rectifier/capacitor charge and discharge states.*

Charging:

$$v_{rect} = R_{total} \cdot i_{in} + L_{total} \cdot \frac{di_{in}}{dt} + v_{dc} \tag{3.2}$$

$$i_{in} = C_{dc} \cdot \frac{dv_{dc}}{dt} + \frac{v_{dc}}{R_{eq}} \tag{3.3}$$

Discharging:

$$v_{dc} = v_{start} \cdot e^{\frac{-t}{R_{eq}C_{dc}}} \tag{3.4}$$

where: R_{eq} is inverter and motor equivalent resistance, and v_{start} is the capacitor voltage at the start of the discharge period.

3.10.2 Implementation of analytical model in MatLab

It was shown in the previous section that the single-phase bridge rectifier may be described by differential equations representing the charge and discharge periods/states of operation. A MatLab code was developed based on these differential equations, to produce an analytical model of the single-phase bridge rectifier. This code is now discussed, with the code found in Appendix B.2.

As with ASD analytical model, the operation of analytical model of the single-phase bridge rectifier is based around an if statement, which compares the value of v_{dc} with v_{rect}. If v_{dc} is

greater than v_{rect}, the discharge expression (3.4) is solved for one time step. This expression is used to calculate the next value of v_{dc}, which is then compared to v_{rect} again in a looped process. In this way, the discharge profile of C_{dc} is found. When the capacitor voltage reduces to a values lower than v_{rect}, the differential equations (3.2) and (3.3), describing the charging period of the rectifier, are solved. These equations return both v_{dc} and i_{in}, and are solved for the period where i_{in} is greater than zero. This gives the 'charging pulse' of the rectifier current. After the charging period, the discharge equation is solved again until the code time step reaches half a cycle. At this point, because the rectifier exhibits a half-cycle symmetry, the process described above is repeated with the known start value of v_{dc}, which is the last value from the previous half-cycle. The value of R_{eq} is updated using the rms values of v_{dc} from the previous half cycle. The circuit is assumed to reach steady state when the difference between the currently calculated value of R_{eq} is no more than 0.1% different than the previous value. In this way, the input current waveform of single-phase rectifier is produced. The operation of the code is illustrated by a flow chart in Figure 3.21.

3.11 Validation of analytical SASD model for sinusoidal and non-sinusoidal supply conditions

In order to fully validate the developed analytical SASD model, comparisons are made between the input current waveforms and associated harmonics predicted by the analytical model and full PSpice SASDs model. The SASD used in this analysis was the V/Hz open-loop SASD controlling 1HP three-phase motor. As before, four different motor loading conditions are considered. Minimum, nominal and maximum values of dc link filter components were selected as presented in Sections 3.5 and 3.6. Both sinusoidal and non-sinusoidal input voltages are applied, with the magnitude of these voltage waveforms varied from 0.8 to 1.2pu, in order to find the P-V and N-V characteristics of the two models.

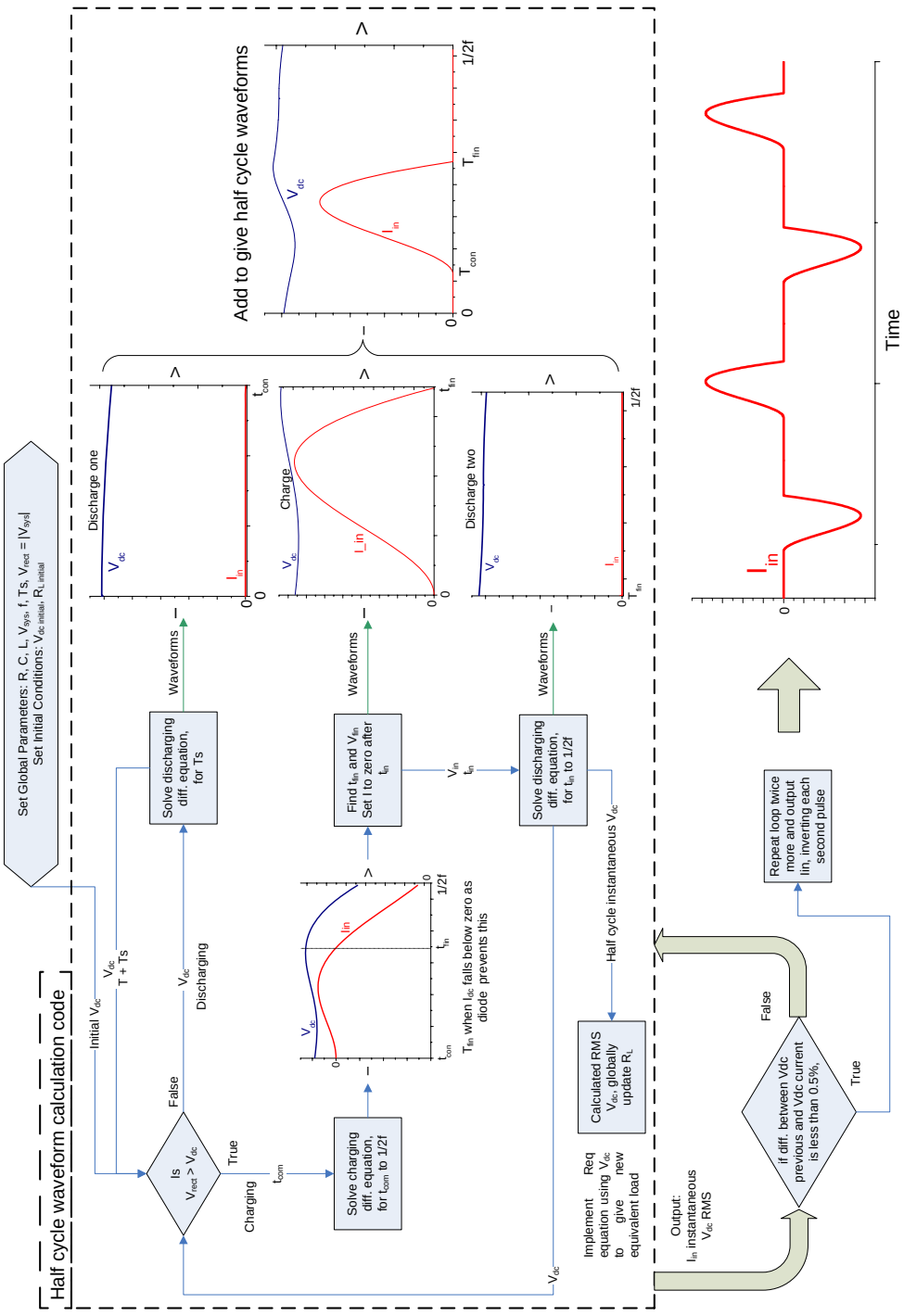
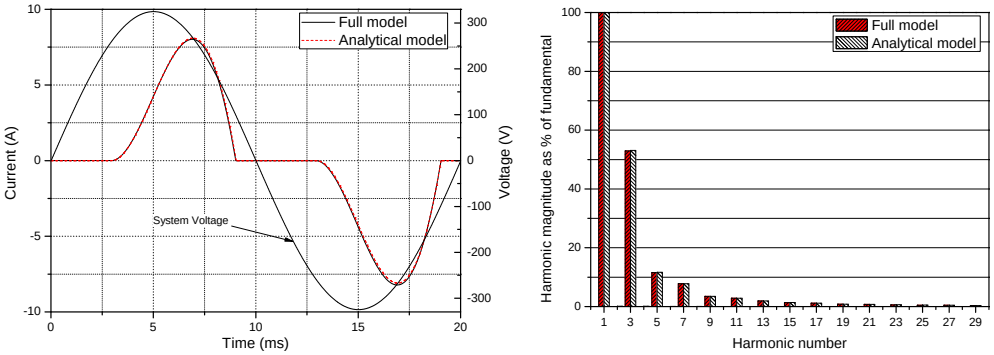


Figure 3.21: *Diagrammatic representation of analytical SASD model.*

3.11.1 Sinusoidal supply conditions

The results of this analysis for a motor mechanically loaded with constant torque are shown in Figures 3.22 and 3.23. Figure 3.22 shows the current waveforms and associated harmonics of the two models at 1pu system voltage with nominal values of dc link filter components. Figure 3.23 shows a comparison of the P-V and N-V characteristics of the two models for minimum, nominal and maximum values of dc link filter components. The results for the motor mechanically loaded with the other considered loads can be found in Appendix B.3.



(a) Current waveforms (b) Harmonics

Figure 3.22: *Comparison between full and analytical model of SASD with applied 1pu sinusoidal system voltage and constant torque mechanical load.*

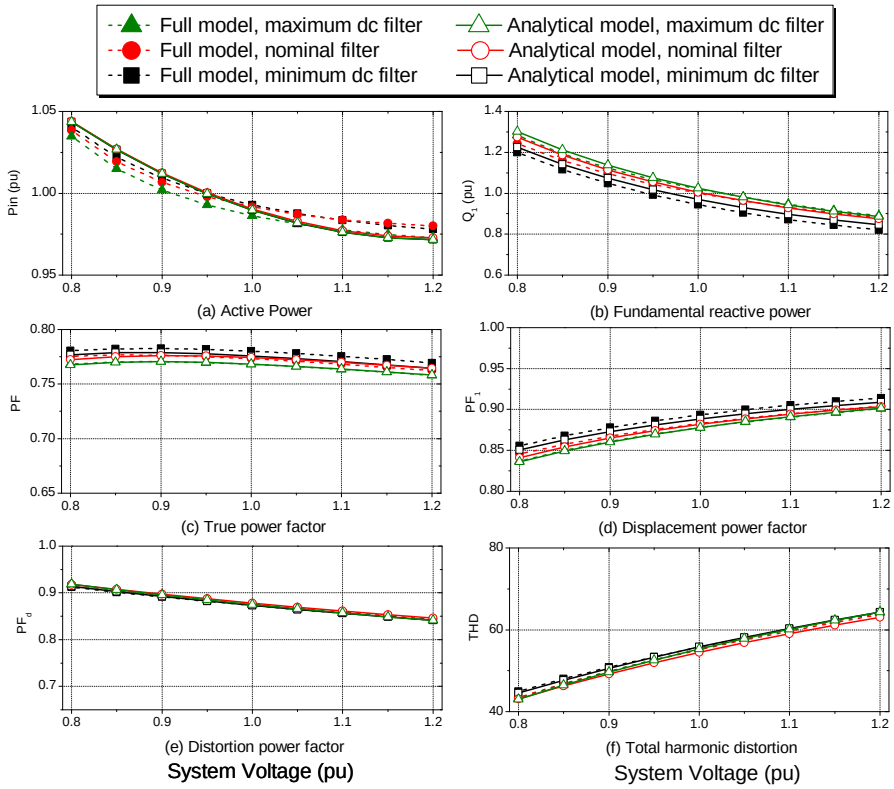


Figure 3.23: *Comparison between characteristics of full and analytical models of SASD with constant torque for min, nom and max dc link component values.*

The results presented in Figure 3.22 show that the proposed analytical model is able to almost exactly predict the shape of the input current waveform of the full PSpice SASD model. Accordingly, the analytical model is also able to represent the harmonic content of full SASD model input current with no significant error. Further, from Figure 3.23 it can be seen that the analytical model will continue to provide this good matching for different system voltages and three selected values of dc link components.

The P-V characteristics of the SASD, Figure 3.23(a), show that the value of the SASD's dc link filter components will have little effect on these characteristics. This was also the case for the previously considered ASD load.

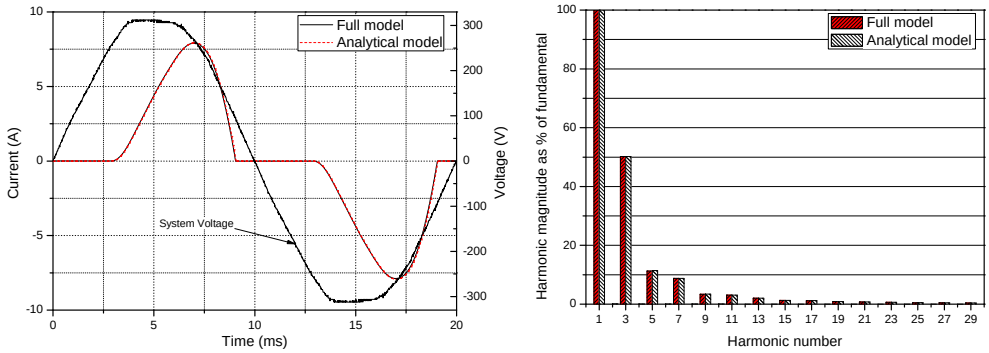
Finally, it can be seen from Figure 3.23(b) and (d) that the fundamental reactive power characteristics of the SASD are also very similar for the considered range of dc link filter components. This result is unlike the result presented for the ASD, were these characteristics where considerably different. The similarity in SASD Q_1-V characteristics is due to the value of L_{dc} in the SASD. As can be seen from Figure 3.7, the value of L_{dc} for the considered SASD (746W) is large and exhibits little variance between minimum and maximum values of C_{dc}. Hence, L_{dc} will dominate the non-active power characteristics of the considered SASD, with the value of C_{dc} having only a very small effect on these characteristics. Furthermore, the difference between nominal and maximum and nominal and minimum values of L_{dc} is greater than the expected variation in typical system inductance. Therefore it can be concluded that alteration in the value of system impedance will have little effect on the characteristics of considered SASD, due to the dominating effect of the passive PFC inductor L_{dc}. However, it is important to note that in lower power SASDs the value of L_{dc} will be much smaller or even zero. Therefore, Q_1-V characteristics will show much more variation with both values of C_{dc} and system impedance. Lower power SASD are considered further in Section 3.12.

The presented results have provided validation of the ability of the analytical model to predict harmonic and power demand characteristics of the SASD with applied constant mechanical torque, under sinusoidal voltage conditions. The results presented in Appendix B.3 further validate the analytical model of SASDs for applied linear torque, quadratic torque and constant mechanical power loading conditions.

3.11.2 Non-sinusoidal supply conditions

The characteristics of the full and analytical models of the SASD with applied non-sinusoidal voltage are now considered. This analysis is performed in order to both validate the analytical model under non-sinusoidal situations, and to further investigate the characteristics of SASDs under these conditions. Again, two non-sinusoidal voltages are applied to the models, termed "typically distorted" and "heavily distorted" (see Section 2.12.2). The results of this analysis

are presented in Figures 3.24 to 3.27.



(a) Current waveforms (b) Harmonics

Figure 3.24: *Comparison between full and analytical model of SASD, with applied"typically distorted" system voltage with magnitude 1pu.*

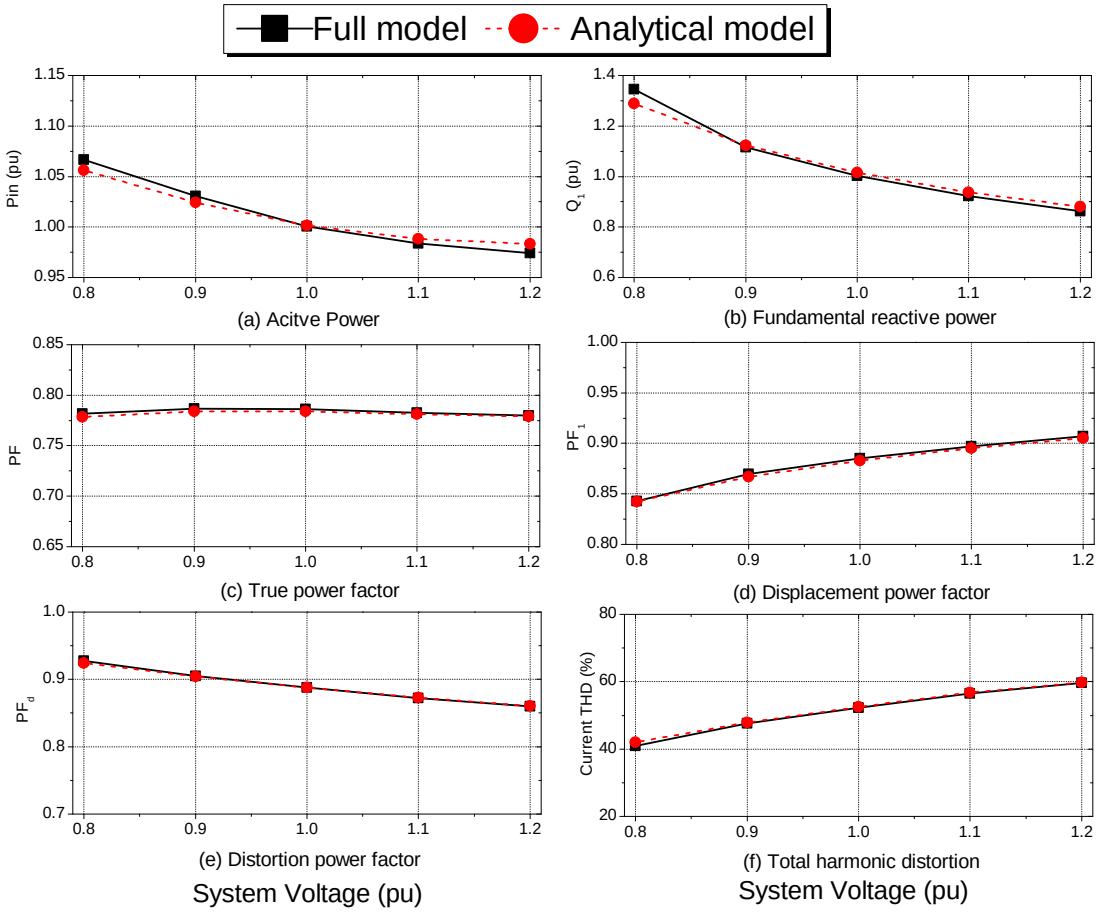
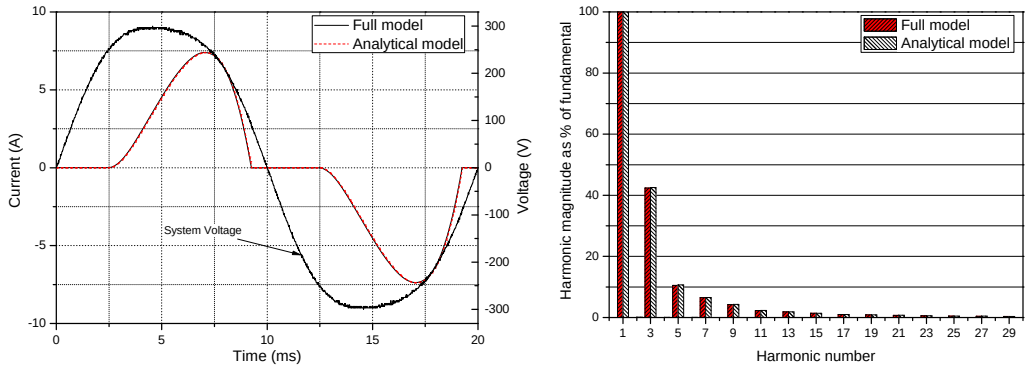


Figure 3.25: *Comparison between characteristics of full and analytical models of SASD mechanically loaded with constant torque load for nominal dc link component values and applied "typically distorted" system voltage.*



(a) Current waveforms (b) Harmonics

Figure 3.26: *Comparison between full and analytical model of SASD, with applied "heavily distorted" system voltage with magnitude 1pu.*

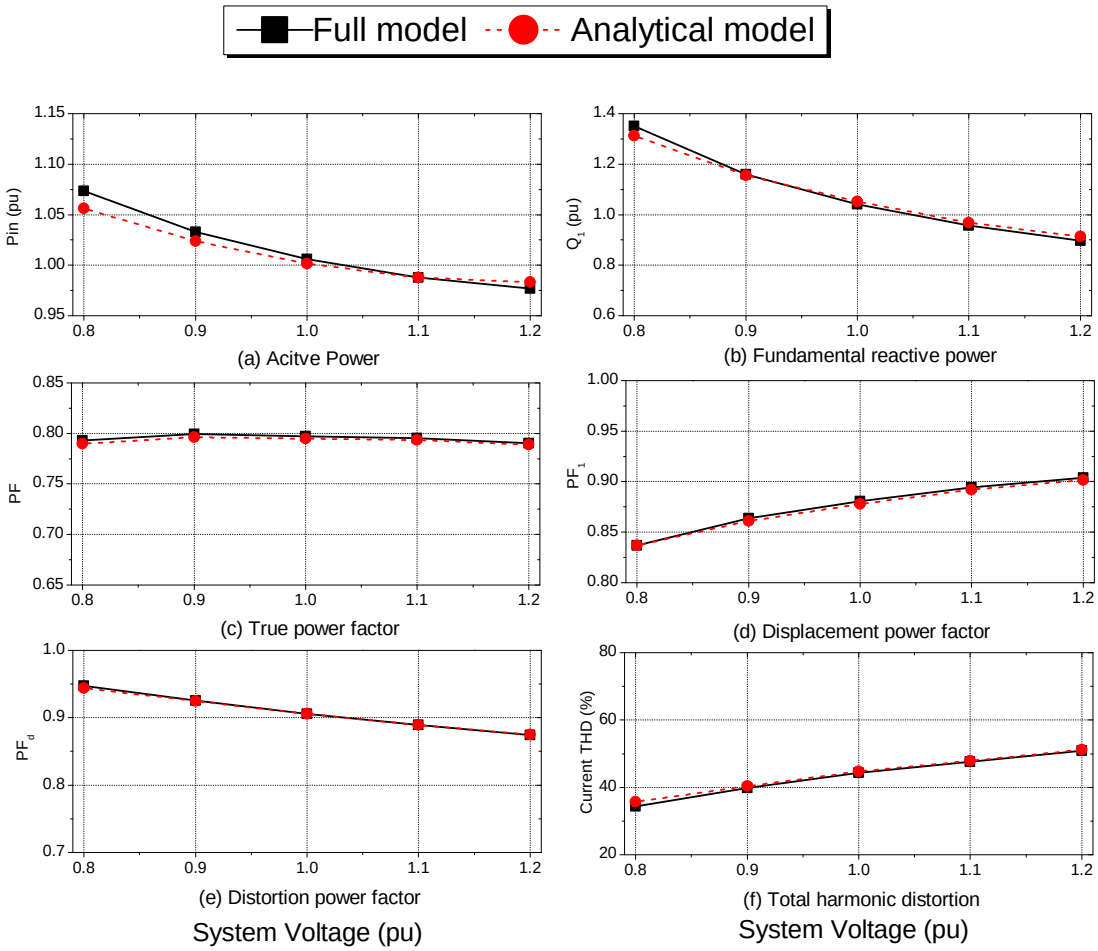


Figure 3.27: *Comparison between characteristics of full and analytical models of SASD mechanically loaded with constant torque load for nominal dc link component values and applied "heavily distorted" system voltage.*

From the results presented in Figures 3.24 and 3.26, it can be seen that the analytical model

can accurately predict the waveshape and harmonic content of the full SASD model input current for both "typically" and "heavily" distorted input voltage conditions. Further, the results presented in Figures 3.25 and 3.27 show that full and analytical models are in good agreement for all considered active and non-active power demand characteristics. Thus, the analytical model may be used to represent the harmonic and power demand characteristics of SASDs in non-sinusoidal supply conditions.

It can also be seen from the presented results that distortion of the system voltage waveform will have no significant effect on the P-V characteristics of the SASD. Further, the Q_1-V characteristics will also be unaffected by distortions in system voltage. This result will be mainly due to the large value of L_{dc} in the considered SASD. Lower power SASDs with smaller values of L_{dc} are expected to show more variation in Q_1-V characteristics for distorted system voltage. Such SASDs are discussed further in the next section.

The results presented in Figures 3.24(b) and 3.26(b) show that distortion in the system voltage waveform will have an effect on harmonic content of the SASD input current. It can be seen that 3^{rd}, 7^{th} and 9^{th} harmonics will slightly decrease with increased input voltage distortion, while the 5^{th}, 11^{th} and higher order harmonics will be relatively unaffected by input voltage distortion. This can also be seen in Figures 3.25(f) and 3.27(f), where the THD of the SASD with applied "typically distorted" waveform is 51% compared to 43% for applied "heavily distorted" waveform. This effect is known as 'harmonic attenuation', [79], and is discussed further in Section 3.12.2.

3.12 Generic analytical model of SASD

It has been shown in this chapter that P-V characteristics of SASDs are essentially independent of the values of SASD dc link filter components and presence of distortion in the applied system voltage. These characteristics, therefore, may be easily represented by polynomial or exponential models. However, the N-V and harmonic characteristics of SASDs will be effected by both values of dc link filter components and distortion of system voltage. Accordingly, an analytical model of SASDs is required to represent these characteristics.

When considering the N-V and harmonic characteristics of an aggregate load of SASD, it is impracticable to form the aggregate load from hundreds or even thousands of individual instances of the SASD analytical model. Therefore, a generic SASD load model is required for representing these aggregate characteristics with a single instance of the analytical SASD model. This generic model is essentially a per-unit representation of the analytical model, able to represent typical SASD characteristics, requiring that C_{dc} and L_{dc} be represented in per-unit form. The value of C_{dc} has already been presented as per-unit values in Section 3.5 and can

be used directly in generic models of SASD. However, the value of L_{dc} in the SASD can not be "generically" represented for all typical rated powers of SASDs. This is because the value of this component is selected based on harmonic limits that are not a function of SASD rated power. As can be seen from Figure 3.7, some SASD, (with rated active power below 380W), will not even require L_{dc}. Therefore, in order to present generic models of SASD, these loads are sub-divided into higher-power SASD and lower-power SASD. The generic models of each of these SASD sub-types are now considered in more detail.

It should be noted that the proposed generic analytical models represent aggregate load made up of same type SASDs, with all SASDs in the aggregate load having nominal parameters and operated at nominal power. The effects of harmonic interactions between same sub-type SASDs due to other than nominal values of parameters, or if operated at other than nominal powers, have not been specifically considered in this thesis.

3.12.1 Lower-power SASD

The lower-power SASD sub-type is selected to represent SASD with rated active power below 380W. This selection is made primarily because SASD below 380W will not require any form of PFC and hence are certain to have different N-V characteristics than SASD that have PFC. Further, it can be seen, from Table 3.1 that the present UK SPIM stock used in refrigerators, chest/upright freezers, fridge-freezers, etc., will usually have rated power below 380W. These are exactly the type of SPIMs that are expected to be replaced with SASDs. As lower-power SASDs will require no PFC, L_{dc} in these loads may be taken as zero, which significantly simplifies the generic model. Therefore, the generic analytical model of lower-power SASDs will have L_{dc} equal zero and C_{dc} as the per-unit value given in Section 3.5 ($X_{C_{dc}}$ = 0.075pu).

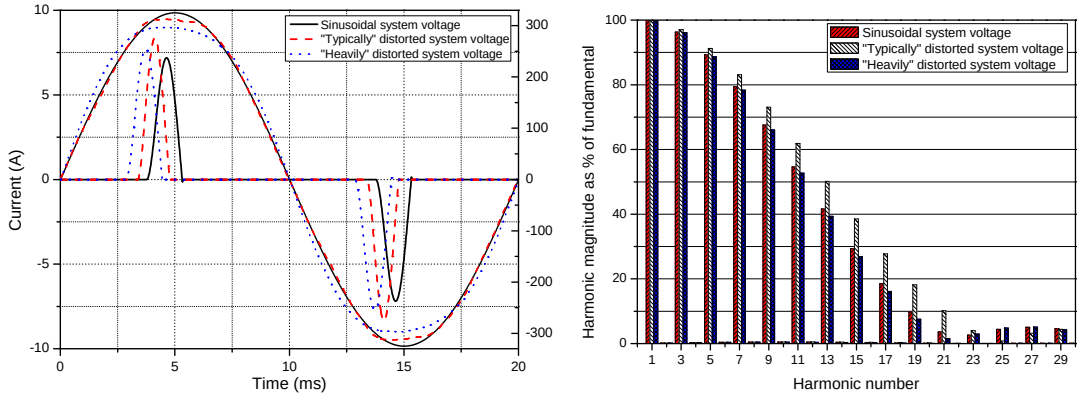
This leaves only the value of R_{in} to be defined in order to form the generic analytical model of lower-power SASDs. The value of this parameter will be dominated by NTC thermistor in the bridge rectifier. The expected value of thermistor resistance is approximately $1 - 2\Omega$ for the thermistor operating in (thermal) steady state, (i.e. "hot"). This is because "hot" resistance values of greater than 2.0Ω will cause excessive losses in the bridge, while "hot" resistance lower than 1.0Ω are unlikely to increase enough when the thermistor is "cold" to provide effective inrush current protection. Accordingly, the typical value of thermistor resistance is taken as 1.5Ω (for "hot"). This value is now converted to a per-unit value for use in the generic analytical model, where a typical base power is taken as 200W. From Table 3.1, this represents roughly the average expected rated power of lower-power SASD. From this, it follows that $R_{base} = \frac{230^2}{200} \approx 265\Omega$, and therefore the per-unit value of $R_{in} = \frac{1.5}{265} \approx 0.0057$pu.

The per-unit values of C_{dc} and R_{in}, along with per-unit expressions for inverter and motor equivalent resistance (from Section 2.10), may be applied directly to the analytical expressions

3.2 to 3.4 to form the generic analytical model of lower-power SASD load-type.

3.12.2 Characteristics of lower-power SASD

The general characteristics of lower-power SASDs are now considered, as they have not been specifically considered elsewhere in this chapter. The developed generic analytical model of the lower-power SASD was used to investigated these characteristics. The model was set-up to represent a 200W lower-power SASD, and the value of system impedance was first altered between minimum and maximum values (see Section 1.8) for applied sinusoidal conditions, in order to quantify the effects of system impedance on lower-power SASDs. Then, the system impedance was set to nominal and “typically” and “heavily” distorted system voltages are applied. As previously, system voltage was varied between 0.8-1.2pu in order to obtain the SASD’ P-V and N-V power demand characteristics. Figure 3.28 shows the input current waveforms and associated harmonics of the lower-power SASD with applied 1pu sinusoidal system voltage, as well as, ”typically” and ”heavily” distorted system voltages. Figure 3.29 shows the P-V and N-V power demand characteristics for each considered case. The results for P-V and Q_1-V power demand characteristics are presented in per-unit, where base value are absolute values of P or Q_1 at 1pu system voltage for each considered case. In this way, the differences or similarities in shapes of the characteristics, specifically the Q_1-V power demand characteristics, may be better seen.



(a) Current/voltage waveforms (b) Current harmonics

Figure 3.28: *Lower-power SASD input current waveforms and associated harmonics with applied, sinusoidal, ”typically” distorted and ”heavily” distorted system voltage.*

It can be seen from Figure 3.29 that P-V power demand characteristics of lower-power SASDs will be unaffected by the changes in system impedance or applied distorted system voltage, as was the case for higher-power SASDs. Figure 3.29, shows that system impedance will have an effect on all N-V power demand characteristics of the lower-power SASD. However, the effect on Q_1-V characteristics is relatively small in absolute terms as fundamental power factor

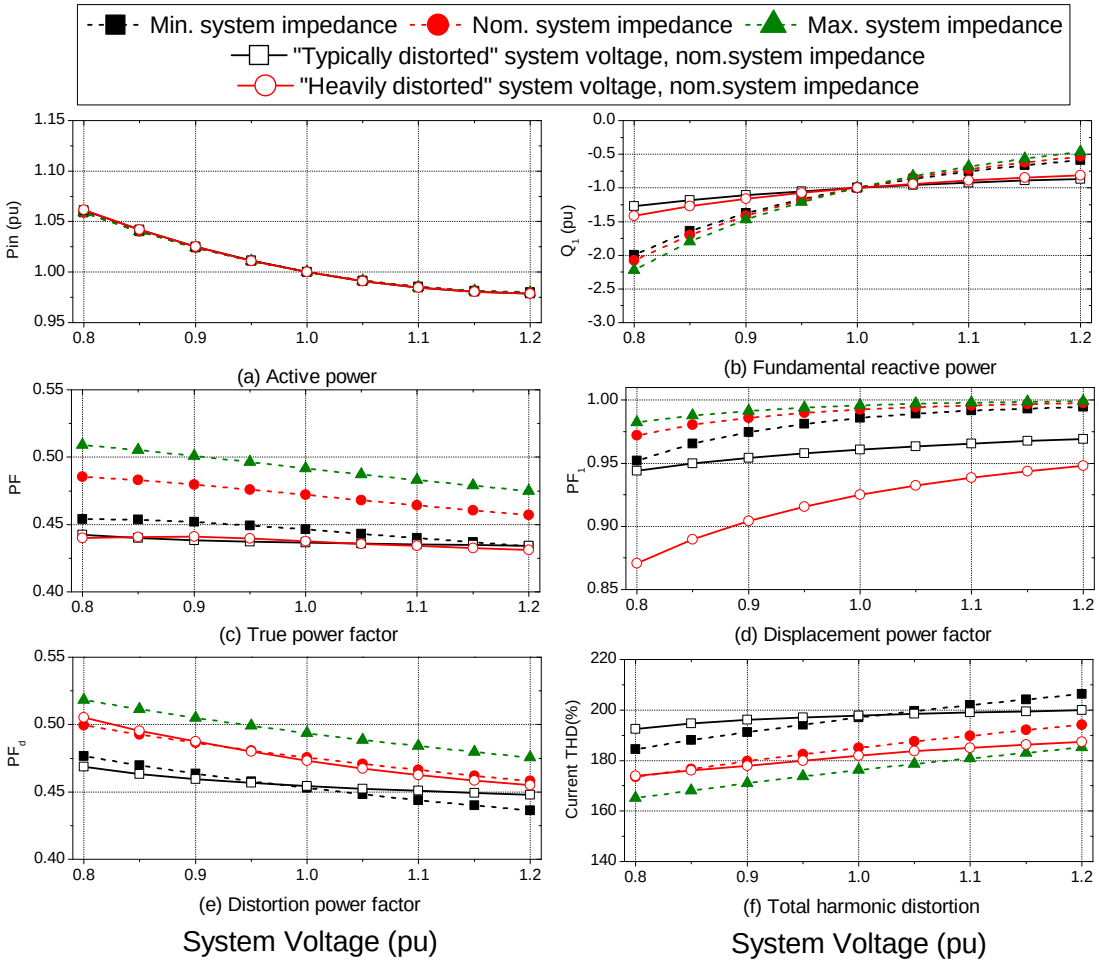


Figure 3.29: *Lower-power SASD P-V and N-V power demand characteristics with minimum, nominal and maximum values of system impedance, for sinusoidal system voltage, and nominal system impedance for"typically distorted" and "heavily distorted" system voltage.*

is close to unity and therefore the absolute value of Q_1 will be small. The effect on SASD' current THD is more significant, with THD varying in a range of approximately 30% between minimum and maximum values of system impedance (lowest value for maximum system impedance). As discussed previously, these effect will not occur in higher-power SASDs, as the large passive PFC inductor will dominate the N-V power demand characteristics of these load sub-types.

It should also be noted that the harmonic content of the lower-power SASD load is very high, as is illustrated in Figure 3.29(f). This high harmonic content is because this load sub-type is not required to meet any specific harmonic legislation, and therefore does not include any form of power factor correction. The implications of this high harmonic content on the supply system are considered later in Chapter 6.

The results of the presented analysis also show that distortion of the system voltage will lead to a significant reduction in lower-power SASD' displacement power factor, (from ≈ 0.99 for sinusoidal supply conditions, to ≈ 0.92 for "heavily" distorted supply conditions. Furthermore, polynomial and exponential models are unable to represent this effect). Additionally, the harmonic content of the lower-power SASD input current waveform will change somewhat with distortion of the system voltage, which is known as "harmonic attenuation". In order to explain these changes in characteristics Figure 3.30 shows the input current and dc link voltage, v_{dc}, of the considered SASD with applied sinusoidal, "typically distorted" and "heavily distorted" system voltage.

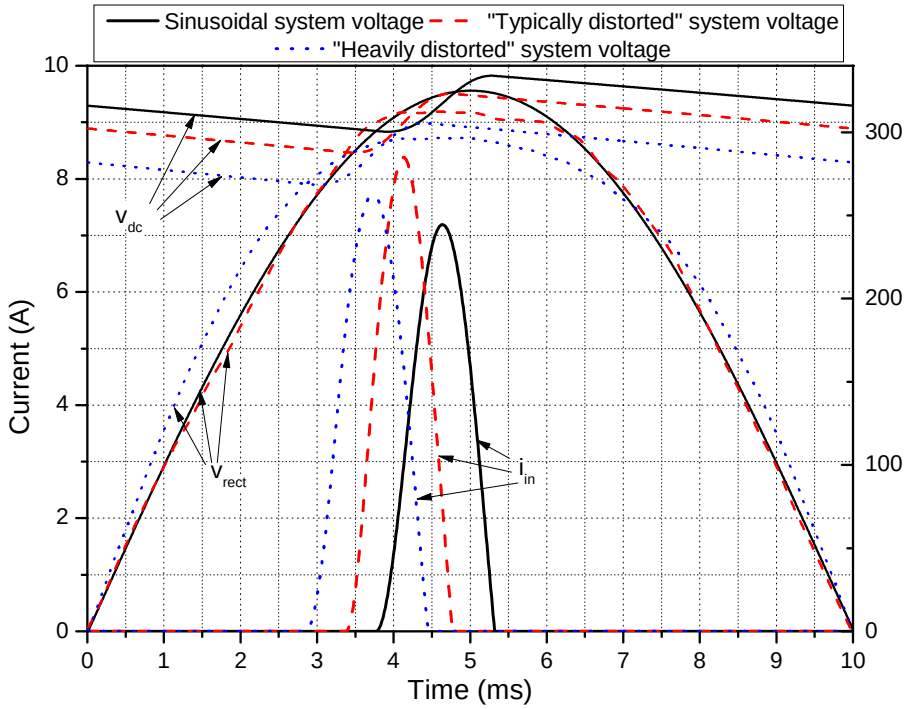


Figure 3.30: *Investigation into the change of characteristics of lower-power SASD with application of distorted supply voltage.*

From Figure 3.30 it can be seen that as system voltage becomes distorted the SASD' dc link voltage, v_{dc}, will reduce and 'meet' the rectified system voltage, v_{rect}, earlier in the associated voltage half cycle. This will influence that the rectifier charging pulses are shifted to the left, what will reduce SASD input displacement power factor and make the SASD load become more capacitive. When the dc link capacitor, C_{dc}, in the SASD is being charged, its rate of charge will be dictated by the conduction path impedance and the difference between v_{dc} and v_{rect}. Therefore, if the system voltage waveform, and hence v_{rect}, is distorted, this will have significant effect on the rate of charge of C_{dc}, influencing the shape of the input current pulse and its harmonic content.

Harmonic attenuation has been considered in [79] and [80]. In these references, it is stated that the single-phase power electronic loads will reduce their harmonic content when system

voltage is "typically distorted" (i.e. characteristic 'flat-top' voltage waveform). While it can be seen from the presented results that for "heavily distorted" system voltage current THD of the lower-power SASD will decrease very slightly, the results also show that the current THD will be greater in "typically distorted" conditions than in sinusoidal conditions. This is because of the particular shape of the selected "typically distorted" voltage in this work, which is not an exact 'flat-top' voltage, but a more realistic waveform which was obtained from actual measurements, as discussed in Section 2.12.2.

Therefore, often made assumption, that the harmonic content of power electronic load will reduce with system voltage distortion should be taken with care, as it is has been shown that the harmonic content of the considered SASD is extremely sensitive to the exact shape (i.e. not to general shape) of the system voltage waveform.

3.12.3 Higher-power SASD

Generic models of higher-power SASDs are more problematic than those of lower-power SASDs, due to the presence of L_{dc} in higher-power SASDs. From the results presented in Figure 3.7, it can be seen that as the rated power of the SASD increases, so does the value of L_{dc}. Thus, there is no typical value, i.e. no common per-unit value, of L_{dc} in SASDs that can be used to represent all of these loads. Accordingly, a typical rated power of these SASDs must be selected in order to define the per-unit value of L_{dc} in the generic higher-power model.

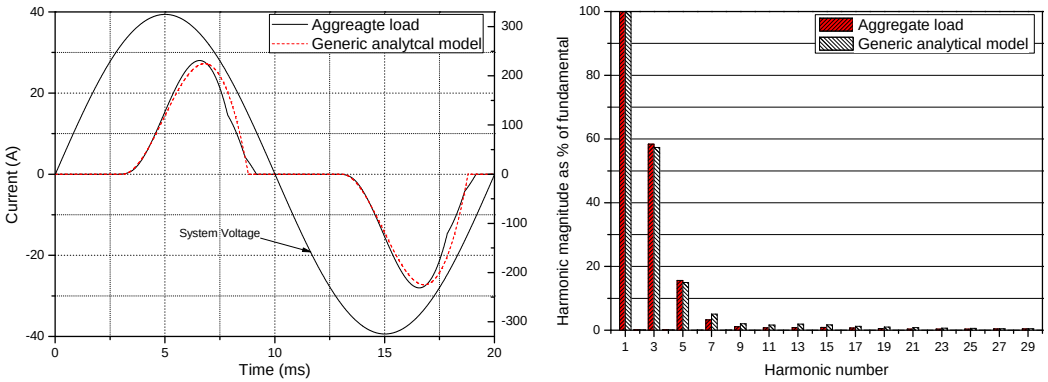
In this work, the typical rated power of higher-power SASD is taken as 850W. This value is chosen as higher-power SASD are likely to be found in applications such as domestic air conditioners and building pumps/fans. It is unlikely that SASD of power much below 850W will be used in these applications, and if these applications require more than 850W, it is likely that 3-phase ASDs will be used instead. Thus, from Figure 3.7, a typical value of 17.5mH is taken for the generic model of higher-power SASD. Expression (3.5) can then be used to convert this typical value of L_{dc} to a per-unit reactance, giving $X_{Ldc} \approx 0.1$ pu.

$$X_{Ldc} = \frac{L_{typical} \cdot \omega}{\left(\frac{V_{nom}^2}{P_{typical}}\right)} = \frac{0.0175 \cdot 2 \cdot \pi \cdot 50}{\left(\frac{230^2}{850}\right)} \approx 0.1pu \tag{3.5}$$

where: X_{Ldc} is the per-unit reactance of L_{dc} in the generic higher-power SASD model, $L_{typical}$ and $P_{typical}$ are the inductance and rated power of selected typical SASD, i.e 17.5mH and 850W.

In order to investigate the error incurred due to this assumption, an aggregate load was formed from 700W, 800W and 900W SASDs, with the value of L_{dc} in each SASD obtained

from Figure 3.7 and C_{dc} taken as nominal for the considered rated powers. A sinusoidal system voltage was applied to this aggregate load with magnitude varied from 0.8 to 1.2pu, in order obtain P-V and N-V characteristics. The proposed generic analytical model of higher-power SASDs was then set to represent an aggregate load of 2400W, and its P-V and N-V characteristics are found. Figures 3.31 and 3.32 compare the characteristics of the aggregate load and those predicted by the generic analytical model.



(a) Current waveforms (b) Harmonics

Figure 3.31: *Comparison between aggregate load formed from 700W, 800W and 900W SASDs and generic analytical model, at 1pu system voltage.*

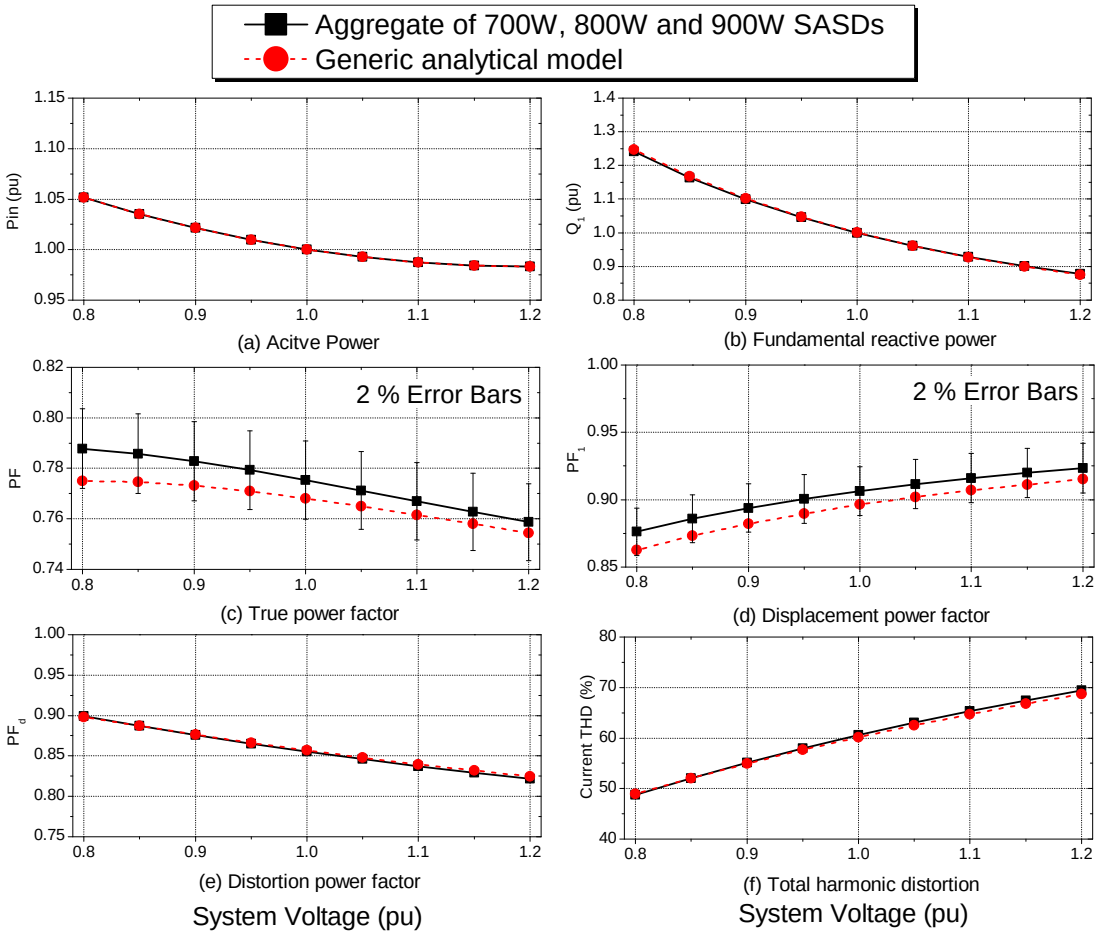


Figure 3.32: *Comparison of power demand characteristics between aggregate load formed from 700W, 800W and 900W SASDs and generic analytical model, at 1pu system voltage.*

The results shown in Figures 3.31 and 3.32 illustrates that there is some error between the predicted aggregate load by the generic analytical model and the actual aggregate load. This error, as discussed before, is due to the selection of a single per-unit reactance value of L_{dc} to represent all SASD in the considered higher-power range.

From Figure 3.32(f) it can be seen that the overall harmonic content of the aggregate and generic analytical models are almost the same. This is because although there is a slight error in prediction of the higher order harmonics, Figure 3.31, the 3^{rd} and 5^{th} harmonics match well, and these harmonics have considerably larger magnitudes compared to the higher order harmonics. This further shows that the large passive power factor inductor in higher-power SASDs will dominate this loads harmonic characteristics, with small changes in value of L_{dc} having very little effect on these characteristics.

As expected, the P-V characteristics of the aggregate load and generic analytical models are

the same, as are their Q_1-V characteristics. Although the generic analytical model predicts a slightly higher demand for fundamental reactive power, as it predicts a lower displacement power factor, this error is small. Therefore, the proposed generic model may be used to represent the considered aggregate load made of higher-power SASDs with acceptable error.

3.13 Polynomial and exponential models of SASD

Now that generic analytical models for lower-power and higher-power SASDs have been developed and verified, polynomial and exponential expressions may be fit to their P-V and Q_1-V characteristics. The corresponding polynomial and exponential model coefficients are derived from relevant generic analytical models with applied sinusoidal system voltage and nominal values of system impedance. These polynomial and exponential model coefficients of the SASDs load type are shown in Table 3.5. Table 3.6 shows the previously presented polynomial and exponential model coefficients for SPIMs in order that the differences between these two load types may be more easily compared. It should be noted that for the lower-power SASDs the polynomial coefficients for reactive power sum to minus 1, to indicate negative reactive power, i.e. capacitive load. There is no such mechanism to distinguish between capacitive and inductive loads in the exponential load model. As the active power demand characteristics of both lower and higher power SASD loads are the same as those of lower-power ASDs, the polynomial and exponential models will also be the same and these models can accordingly be seen in Figure 2.56. The Q_1-V characteristics of SASDs and ASDs will however not be the same, and Figures 3.33 and 3.34 show comparison between SASD generic analytical, polynomial and exponential models. Once more, it can be seen that the presented polynomial models will show better matching than the exponential models, especially for fundamental reactive power elements. There were no previous models of SASDs found in literature, so no comparison with existing models can be made here.

It should be noted that polynomial and exponential models can not represent the discussed variation in lower-power SASD N-V power demand characteristics with distortion of system voltage and smaller variations with change in system impedance. The higher-power SASD shows much less variation due to system voltage distortion and essentially no variation for different system impedances, so polynomial and exponential models are more valid for expressing the general characteristics of this load sub-type even under distorted system voltage conditions.

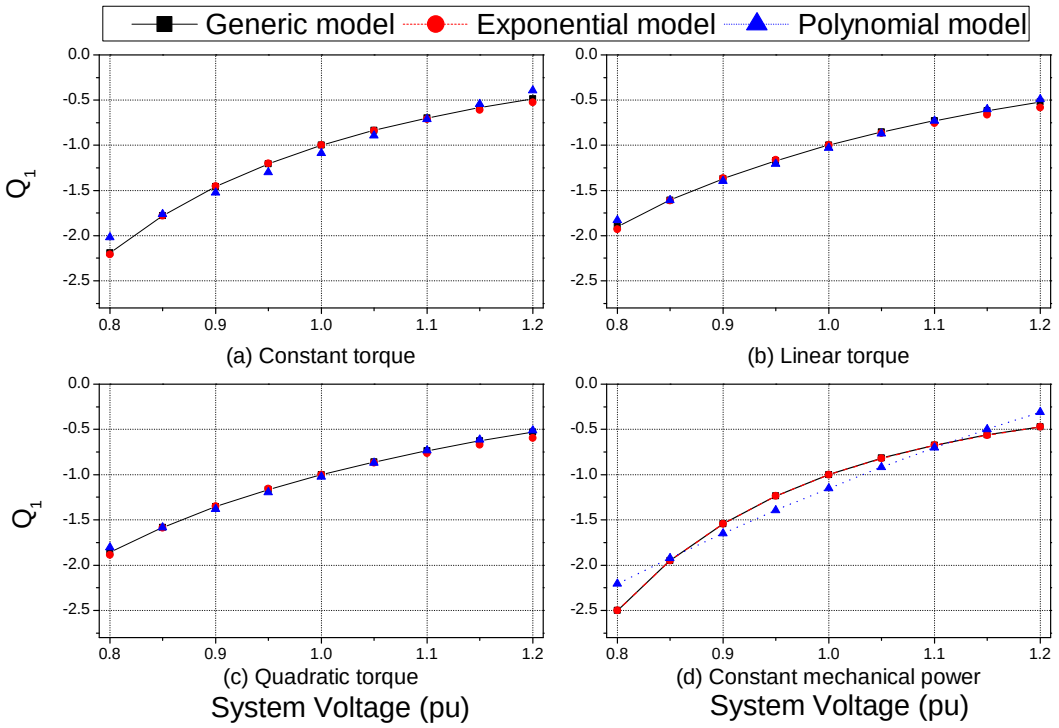


Figure 3.33: *Results obtained using proposed exponential and polynomial models of lower-power SASDs, fundamental reactive power.*

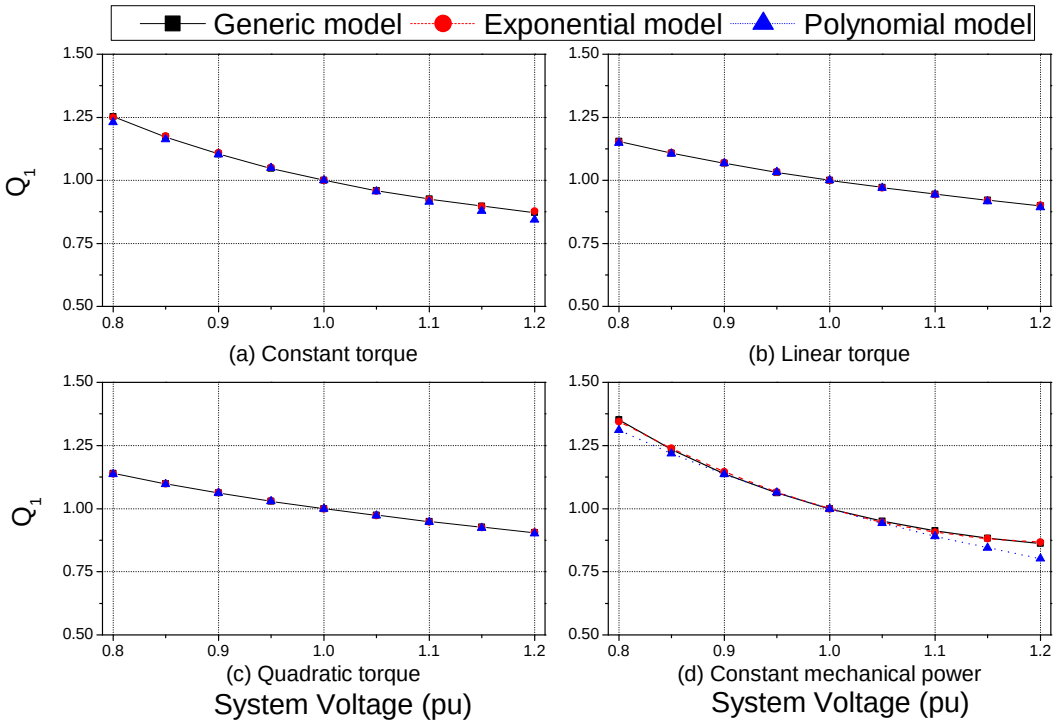


Figure 3.34: *Results obtained using proposed exponential and polynomial models of higher-power SASDs, fundamental reactive power.*

Table 3.5: *Proposed exponential and polynomial model coefficients of SASDs.*

Loading	PF_1	Exp. Model		Polynomial Model					
		np	nq	Z_p	I_p	P_p	Z_q	I_q	P_q
Higher power V/Hz open-loop SASDs									
CT	0.896	-0.10	-0.88	0.40	-0.89	1.49	1.54	-3.95	3.41
LT	0.896	0.08	-0.71	0.02	0.0	0.98	0.95	-2.60	2.66
QT	0.896	0.22	-0.57	-0.27	0.76	0.51	0.54	-1.65	2.11
CP	0.896	-0.19	-1.11	1.08	-2.5	2.42	2.47	-6.04	4.56
Higher power V/Hz closed-loop SASDs									
all	0.896	-0.19	-1.11	1.08	-2.5	2.42	2.47	-6.04	4.56
Higher power advanced controlled SASDs									
all	0.896	0	-0.73	0	0	1	1.45	-3.66	3.19
Lower power V/Hz open-loop SASDs									
CT	0.99	-0.10	-3.33	0.40	-0.89	1.49	-3.32	10.50	-8.18
LT	0.99	0.08	-2.72	0.02	0.0	0.98	-3.65	10.34	-7.69
QT	0.99	0.22	-2.63	-0.27	0.76	0.51	-3.67	10.31	-7.64
CP	0.99	-0.19	-3.91	1.08	-2.5	2.42	-3.02	10.62	-8.60
Lower power V/Hz closed-loop SASDs									
all	0.99	-0.19	-3.91	1.08	-2.5	2.42	-3.02	10.62	-8.60
Lower power advanced controlled SASDs									
all	0.99	0	-2.81	0	0	1	-3.61	10.39	-7.78

Table 3.6: *Proposed exponential and polynomial model coefficients of SPIMs, (as previously presented).*

Loading	PF_{nom}	Exp. Model		Polynomial Model					
		np	nq	Z_p	I_p	P_p	Z_q	I_q	P_q
RSIR CT	0.62	0.06	1.92	0.63	-1.20	1.57	1.40	-0.91	0.50
RSIR LT	0.62	0.19	1.92	0.31	-0.43	1.11	1.40	-0.91	0.50
RSIR QT	0.62	0.30	1.92	0.10	0.10	0.80	1.40	-0.91	0.50
RSIR CP	0.62	-0.12	1.92	1.16	-2.42	2.26	1.40	-0.91	0.50
RSCR CT	0.90	0.38	1.68	0.50	-0.62	1.11	1.54	-1.43	0.89
RSCR LT	0.90	0.46	1.68	0.34	-0.22	0.88	1.54	-1.43	0.89
RSCR QT	0.90	0.53	1.68	0.22	0.08	0.69	1.54	-1.43	0.89
RSCR CP	0.90	0.29	1.68	0.73	-1.16	1.43	1.54	-1.43	0.89

3.14 Conclusions

This chapter has identified and reviewed typical types of single-phase induction motors used in residential and commercial applications. Detailed models of these motors have been developed from existing motor theory. These models have then been used to investigate active and reactive power demand characteristics of these loads with changes in system steady state voltage. The analysis has shown that P-V characteristics of SPIMs are dependent on the type of motor and the type of mechanical load the motor is driving. The analysis has also shown that the Q-V characteristics of SPIMs are dependent on type of SPIM, but are essentially independent of type of motor mechanical loading. As SPIM are linear loads, their polynomial and exponential models are proposed to accurately represent their P-V and Q-V characteristics. The proposed SPIM load models are generally in good agreement with previously presented load models. Rather than presenting these models based on specific type of motors, they have been presented based on type of motor mechanical loading. In this way, flexibility has been provided, as the developed models may be used to represent a wide range of motors used in a variety of end-use applications.

In the future, SPIMs are expected to be partly replaced by more efficient single-phase drive-controlled motors (SASD). Therefore, detailed models of typical SASDs have been developed in this chapter. Analyses of these models have revealed that the P-V characteristics of SASD loads are essentially the same as those presented previously for lower-power ASD load. However, the N-V and harmonic characteristics of SASDs loads are significantly different than those of lower-power ASDs. It has been shown that these characteristics will be dominantly dictated by the values of the SASD's dc link filter components, L_{dc} and C_{dc}. Thus, an analytical model of SASD has been developed and validated for both sinusoidal and non-sinusoidal supply system voltages.

Typical per-unit values of C_{dc} for SASDs have been derived and presented. It has been found that the value of L_{dc} will be dictated by EU harmonic standards. These standards set absolute limits on allowable harmonic currents for individual SASD load. These limits are independent of rated power of the SASD load. It has been shown that these standards will have a profound influence on the non-active and harmonic characteristics of the SASD. This influence is to such an extent, that the SASD load category has to be sub-divided into two load sub-types: lower-power and higher-power SASDs. Lower-power SASD load is capacitive, while higher-power SASD load is inductive. The THD of lower-power SASDs is high, typically 190%, compared to 60% of higher-power SASDs. Thus, lower-power SASDs are expected to have significant influence on supply system harmonics, as is further investigated in Chapter 6. The displacement power factor of lower-power SASD will also be significantly affected by system voltage distortion, which in turn will influence the fundamental reactive power supplied by this load to the supply system.

Generic models of each of the SASD load sub-types have been derived from the developed analytical SASD models. These generic load models may be used directly in aggregate system load models to represent the components of SASD load. Finally, for the completeness of the discussion, polynomial and exponential SASD models have been presented, which can also be used directly in power system studies (e.g. standard load flow analysis) where the harmonic characteristics of the load are not considered important.

Chapter 4
Electronic dc power supply loads

4.1 Introduction

This chapter focuses on developing load models of dc power supplies found mainly in domestic applications. The most common examples of these loads include: PCs, monitors, televisions, DVD/CD players/recorders, etc. Over the past few decades, the number of these devices in the UK has increased significantly, due to the boom in the consumer electronics market. It is estimated that electronic load are now responsible for around 25% of the total UK domestic electrical power demand, [14] and [81]. This figure is expected to increase by 2020 to around 33% of total UK domestic power demand, [14]. Figure 4.1 shows this increasing trend in energy consumption of electronic loads in the UK domestic sector since 1980.

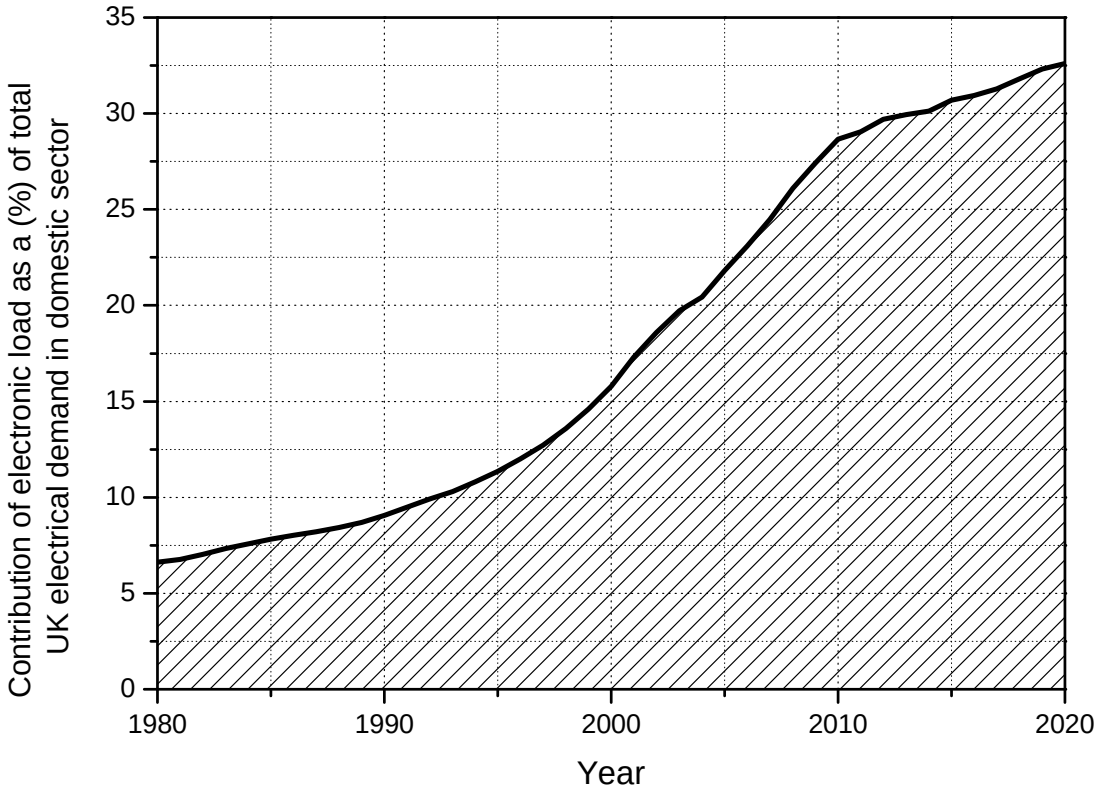


Figure 4.1: *Electrical energy consumption of electronic equipment from 1980-2020, [14].*

Modern electronic dc power supply loads are often referred to as switch-mode power supplies

(SMPS) [1]. They are non-linear loads and introduce harmonics into the supply system. While there has been a fair amount of work into harmonic emissions associated with SMPS, the majority of it has been performed prior to 2001, when new and more stringent harmonic legislation was introduced. This chapter investigates effects of this legislation on characteristics (and load models) of SMPS. From the load modelling point of view, this legislation has led to the creation of two new sub-types of SMPS loads, which have not been considered in previously published literature. It was found that the P-V characteristics of pre- and post- 2001 SMPS are essentially the same, while the harmonic emissions and N-V characteristics are significantly different.

A general SMPS PSpice model of electronic load is developed, in order to obtain full models of SMPS loads. This full model was verified by measurements, and then translated into an equivalent circuit model in the same way as performed for SASD load previously. This equivalent circuit model was then further converted to an analytical model and verified with measurements for applied sinusoidal and non-sinusoidal system voltage conditions. A detailed review of the typical values of relevant circuit components in SMPS was performed, and the obtained data were used to form general analytical models of each SMPS load sub-type. It is shown that the proposed general analytical models are able to accurately represent all power and harmonic characteristics of an aggregate load made up of same sub-type SMPS load. Finally, polynomial and exponential models of each SMPS load sub-type are presented.

4.1.1 Previous work on the representation of electronic loads for power system studies

There has been very little previous work on the representation of electronic loads for power system studies, with only three previous reference presenting models for these loads, [15], [22] and [3]. Reference [22] recommends a general load model for office equipment which consists of PCs, monitors and printers. Reference [15] presents a load model for television load and reference [3] recommends that electronic loads should be represented as constant MVA loads, but does not state load power factor. These models are shown in Table 4.1.

Table 4.1: *Existing model coefficients of electronic loads.*

Loading	PF_{nom}	Exp. Model		Polynomial Model					
		np	nq	Z_p	I_p	P_p	Z_q	I_q	P_q
Electronic load, [3]	-	0	0	-	-	-	-	-	-
Television, [15]	0.8	2	5.1	-	-	-	-	-	-
Office equipment 1 [22],	1.00	0.24	0	0.34	-0.32	0.98	0.00	0.00	0.00
Office equipment 2 [22],	1.00	0.20	0	0.08	0.07	0.85	0.00	0.00	0.00

[1] In this thesis, terms "dc power supply" and "switch-mode power supply (SMPS)" are used interchangeably. Only uncontrolled (unregulated) dc power supplies cannot be termed as SMPS.

Although there has been other research on the characteristics of electronic loads and their effects on the supply system, this previous research has been focussed almost exclusively on their harmonic emissions. The changes in active/reactive power demand characteristics with changes in supply system voltage have not been considered there.

4.2 Components and configurations of electronic dc power supply loads

Electronic equipment requires a dc voltage to operate, and therefore contain electronic circuits (dc 'power supply') for conversion of ac input system voltage to dc voltage. As discussed previously, a single-phase diode bridge rectifier is the standard circuit used for the conversion of ac to dc voltage. Modern electronic circuits are very sensitive to variations in applied dc voltage, and require this voltage to be tightly regulated. The bridge rectifier alone can not provide a constant dc voltage, as its output voltage has a large ac ripple component, unacceptable for supplied electronic circuits. Therefore, an additional circuit, known as a dc-dc converter, is required to stabilise rectifier output voltage, i.e. to regulate it at a value suitable for supplying the back-end dc electronic load. Figure 4.2 shows a block diagram of a typical modern dc power supply, commonly referred to as switch mode power supply (SMPS). The main component blocks of SMPS' load are discussed below. It should also be noted that there may be a few lower-power devices that do not contain dc-dc converters, which are termed here as unregulated dc power supplies. However, these dc power supplies will be of very low rated power, and hence will not have any significant influence/contribution to the overall power consumption of dc power supply loads. Accordingly, they are not considered further in this work.

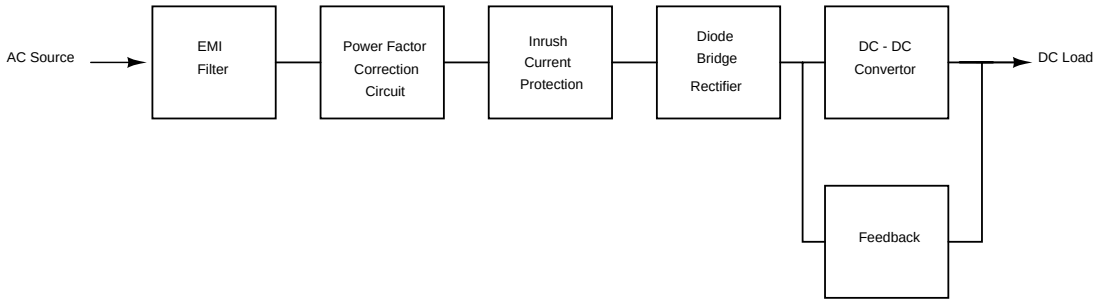


Figure 4.2: *Major components of a typical modern SMPS.*

4.2.1 EMI-filter

The dc-dc converters found in SMPS will operate at high frequency, usually 65kHz-300kHz, (discussed in more detail in Section 4.2.5) and will require an EMI suppression filter to meet the

required standards, [82]. A typical EMI filter commonly found in SMPS is shown in Figure 4.3. It consists of a common mode ("choke") inductance, L_{emi}, combined with a capacitance, C_{emi}. The common mode choke is a bi-filar wound inductor, which acts as a low impedance path for balanced currents (induced fluxes in each coil are cancelled), and as a high impedance for unbalanced currents (fluxes in coils do not cancel). The EMI capacitor also helps to further attenuate the EMI noise, [83]. The value of the choke will depend on the switching frequency and the amount of attenuation required. It is typically small, 50μH to 800μH. The value of the C_{emi} is also relatively small, typically in the range 100nF to 600nF. Because of these small values, the EMI filter is not having any significant effect on the operation of the SMPS from the load modelling point of view.

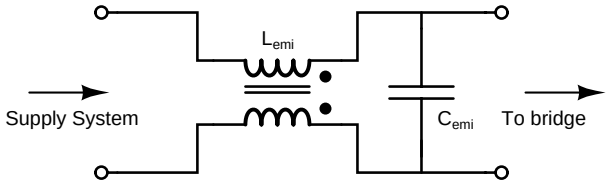


Figure 4.3: *Typical SMPS EMI-filter.*

4.2.2 Bridge rectifier

The operation of the single-phase bridge rectifier circuit has been discussed previously (Section 3.3.1).

The dc link filter capacitor C_{dc} found in the SMPSs is usually selected regarding two essential design criteria: a) allowed dc voltage ripple, and b) required 'hold-up time' [84], [36]. These are discussed further below, where it is shown that the 'hold-up time' requirement will effectively dictate the value of C_{dc}.

Due to harmonic legislation, certain SMPS may also include an inductor in the rectifier circuit, L_{dc}, in order to implement passive PFC (similar to both ASDs and SASD, which also use this method of PFC). The value of L_{dc} will be selected based on meeting specified harmonic limits. Suitable values of this component are discussed in Section 4.4.1, where corresponding harmonic limits are presented.

4.2.2.1 DC link voltage ripple

The ripple of the bridge rectifier output voltage is defined as the difference between the maximum and minimum values of this voltage. Its value will depend on the discharge rate of C_{dc} (i.e. size of C_{dc}) and the power drawn from C_{dc} by the SMPS supplied load. Although the level of acceptable dc link voltage ripple is application specific, it will typically be less than

20% of the nominal dc link voltage, [84]. Expression (4.1) may be used to find the minimum allowed value of C_{dc}, based on the rated power of the SMPS and the allowed dc link voltage ripple.

$$C_{dc} = \frac{P_{SMPS}}{\eta \cdot (v_{rip,max}^2 - v_{rip,min}^2)} \times \frac{1}{f} \tag{4.1}$$

Where: f is frequency of the supply system voltage, P_{SMPS} is the rated active power of the SMPS, $v_{rip,max}$ and $v_{rip,min}$ are the maximum and minimum dc link voltage (i.e. peak and trough values of dc link voltage ripple).

4.2.2.2 Hold-up time

The hold-up time of the SMPS is defined as the time for which dc link voltage will still be within specifications after a full interruption of the supply system voltage. Hold-up time is dictated by legislation, [85], which states that SMPS should have immunity to voltage interruptions of up to 10ms (half cycle). Therefore, if the voltage interruption starts just before the dc link capacitor is about to be charged, then a 10ms interruption can translate into close to a 20ms period for fully charged capacitor. Accordingly, hold-up time around 23ms is commonly used in industry, as it represents the 20ms plus a safety margin ([84], [86], [87]). In order to calculate the size of C_{dc} necessary to achieve a particular hold-up time, the rated power of the SMPS and the minimum operational input voltage of the dc-dc converter in the SMPS must both be known. The difference between the nominal operating voltage of the dc-dc converter and the minimum operating voltage will be dependent on the specific dc-dc converter. However, values of 80-100V are common, [84]. Therefore, a value of C_{dc} that should be selected should be large enough to keep dc link voltage, not less than 80-100V lower than its nominal value, after a full supply voltage interruption. Expression (4.2) may be used to calculate the typical size of C_{dc} required to meet the hold-up time criteria.

$$C_{dc} = \frac{2 \times P_{SMPS} \times t_{hu}}{\eta \times (v_{dc,nom}^2 - v_{dc,min}^2)} \tag{4.2}$$

Where: t_{hu} is the specified hold up time, η is the efficiency of the SMPS, $v_{dc,nom}$ and $v_{dc,min}$ are the nominal and minimum operating voltage of the dc-dc converter.

4.2.3 Estimation of typical size of C_{dc}

Figure 4.4 shows the minimum values of C_{dc} required to achieve 24ms hold-up time for a range of SMPS rated powers, assuming the dc-dc converter can operate for up to a 80V drop

from nominal input voltage, i.e. 230-80=150V (for UK/EU supply systems). Also shown in Figure 4.4 are the values of C_{dc} that would lead to associated dc link voltage ripples of 10% and 20%, and actual values of C_{dc} found in different SMPS'. These values have been obtained from the manufacturers data sheets and through the examination of available SMPS devices.

It can be seen from this figure that these actual values of C_{dc} all lie fairly close to the 23ms hold-up time line. Therefore, it can be concluded that 23ms hold-up time is the main criteria by which the value of C_{dc} in SMPS is selected. Accordingly, per-unit value of $X_{C_{dc}}$ for SMPS loads may be found from the 23ms hold-up time line, using (4.3) and a point from this line (e.g. P_{SMPS} =250W, C_{dc} = 415μF). This is an important result for development of generic SMPS models.

$$X_{Cdc,pu} = \frac{\left(\frac{1}{C_{dc}\cdot\omega}\right)}{\left(\frac{V_{phase}^2}{P_{SMPS}}\right)} = \frac{\left(\frac{1}{415\times10^{-6}\cdot\omega}\right)}{\left(\frac{230^2}{250}\right)} \approx 0.036pu \tag{4.3}$$

where: V_{phase} is the input phase voltage, P_{SMPS} is the rated power of the SMPS, $\omega = 2\pi f$ where f is the system frequency.

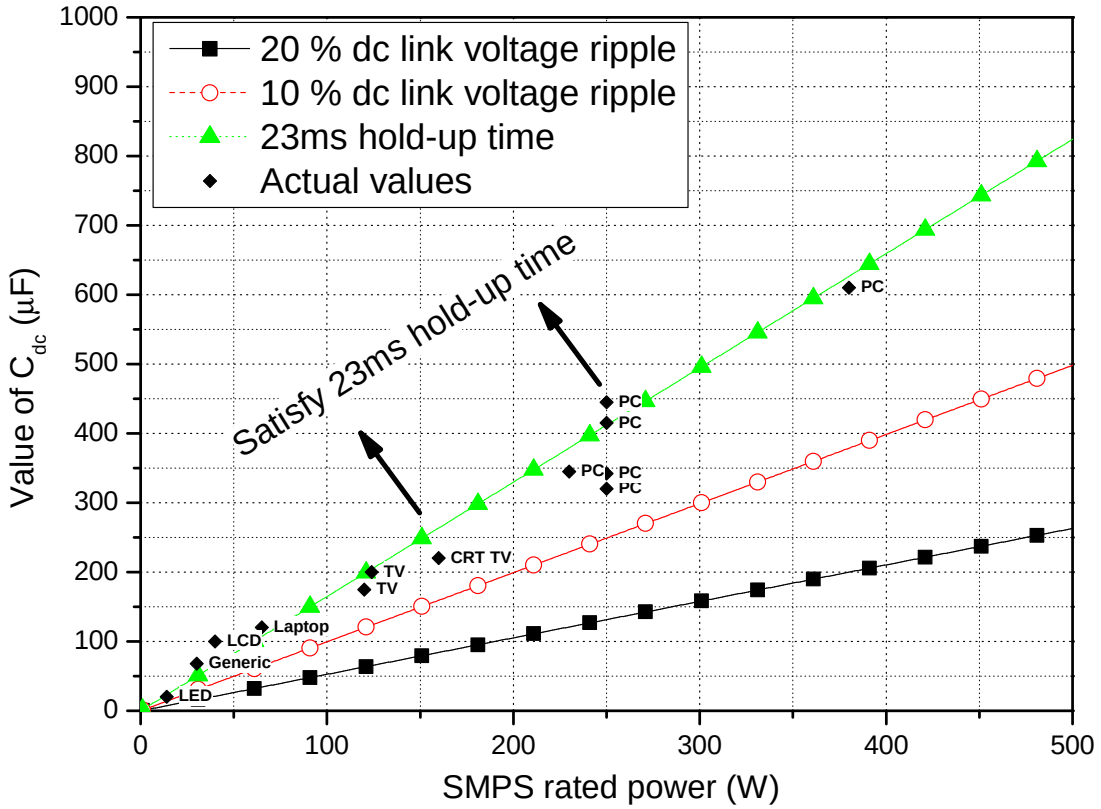


Figure 4.4: *Values of C_{dc} found in SMPS loads.*

4.2.4 Inrush current protection

As SMPS' contain relatively large capacitors ($X_{C_{dc}}$ = 0.036pu), on initial 'switch-on', when dc link voltage is = 0 (or when it is very low), a low impedance path is presented to the supply system and a large current will flow for a short period of time while C_{dc} is charging. This current is commonly known as "inrush current" and, if not limited, may damage the components within the SMPS bridge rectifier.

Two approaches are commonly used by industry to reduce inrush current. These are usually referred to as active and passive inrush current protection. Active inrush current protection can be found in a variety of forms, but will usually consist of components such as triacs, resistors, relays and thyristors. Passive inrush current protection is achieved simply by using a negative temperature coefficient (NTC) thermistor, and is considerably cheaper than the active alternative. It is estimated that over 90% of devices on the market that require inrush current protection use NTC thermistors, [88].

The steady state resistance of the NTC thermistor is proportional to average current flow through the component, with a higher average current resulting in a lower resistance of the thermistor. The NTC thermistor also has a large thermal time constant, with a typical "cool-down period" of around 60 seconds, [88]. In the event of short supply system voltage reduction, this may be problematic, as the thermistor will not cool down sufficiently, and its resistance will stay low, resulting in high in-rush current upon recovery of normal supply voltage. This is discussed in detail in [35], and is of importance for the development of accurate dynamic models of dc power supplies. The characteristics of a typical NTC thermistor are shown in Figure 4.5. With respect to steady-state load modelling of SMPS, the NTC thermistor will introduce additional resistance to the rectifier conduction path.

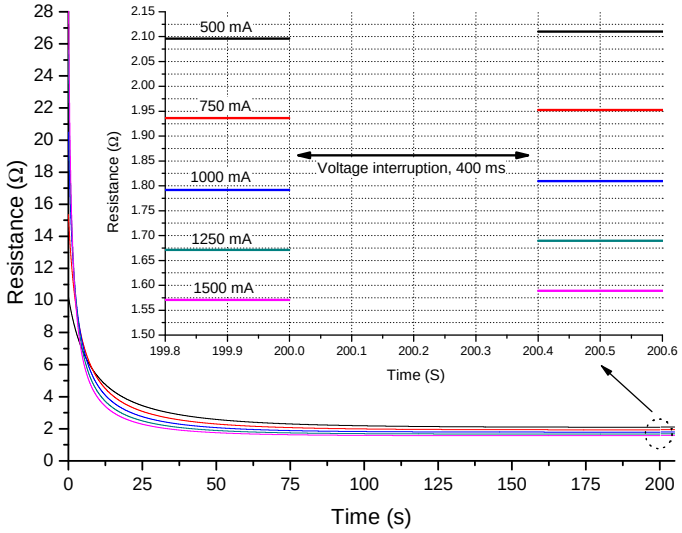


Figure 4.5: *Characteristics of a typical NTC thermistor.*

Another form of active inrush current protection is to include a relay in parallel with the NTC thermistor. This relay is closed when the SMPS is operating, (i.e. when dc link voltage is above a preset level), allowing the NTC to thermistor to cool down. If a voltage interruption occurs, (i.e. dc link voltage reduces to less than preset level) the relay opens and the thermistor is in the rectifier conduction path. On voltage recovery, the "cold" NTC thermistor will act to limit the inrush current.

4.2.5 DC-DC converter

As discussed previously, the function of the dc-dc converter is to stabilise bridge rectifier output dc link voltage, v_{dc}, which has a relatively large ac ripple component. The output of a dc-dc converter is a dc voltage with a low ripple, suitable for electronic equipment/components that are very sensitive to voltage fluctuations. The dc-dc converter must also regulate variations in the input system voltage, which should not be transferred to the electronic components it supplies.

There is a wide variety of dc-dc converters. However, they may be split generally into two categories: forward-mode and flyback-mode converters. Forward-mode converters are usually applied in higher power applications, such as desktop PCs, while flyback-mode converters are applied in lower power applications, such as laptop power supplies. Reference [83] gives full descriptions of the operation of flyback and forward mode converters.

4.2.5.1 General DC-DC converter

Although there are several different topologies of dc-dc converters, they will all act in a similar way, trying to keep their dc output voltage constant when their input voltage changes within a specified range (typically 70% to 120% of nominal voltage). As dc-dc converter output voltage is maintained constant, the active power drawn by the dc-dc converter will also remain constant with change in system voltage. Therefore, for the purposes of load modelling, the exact topology of the dc-dc converter is not important.

4.3 Full PSpice models of SMPS

Following the same methodology as in preceding chapters, PSpice software was used to develop a detailed (i.e. full) model of a typical SMPS with flyback-mode converter. The flyback-mode converter topology was selected as it is one of the most common topologies, and as discussed previously, its performance in relation to regulation of dc output voltage is not different from any other dc-dc converter type.

Although used for developing steady-state models load models, the full SMPS model is of sufficient detail for transient analysis. This is successfully demonstrated in [35], where SMPS models from this thesis are used for the analysis of inrush currents taken by the SMPS during voltage sags. This model is now verified by comparison with measured data.

4.3.1 Full SMPS model

The full flyback-based SMPS PSpice model, shown in Figure 4.6, incorporates a detailed PSpice model of a typical controller chip, [89], which controls the power MOSFET, "flymos". When flymos is on, current builds up in the primary inductance of the flyback transformer L_p (storing the energy), while D5 prevents current flowing into the secondary, L_s. When flymos is switched off, the stored energy is released into L_s. Hence, the output voltage of the converter is controlled by altering the duty ratio of the switching pulses. The output voltage feedback signal is supplied to the controller chip by means of an opto-coupler, which provides isolation between high and low voltages in the SMPS. The implemented bridge diode model is based on the device characteristics found in [35]. The EMI choke, L_{emi}, is represented with a standard PSpice transformer.

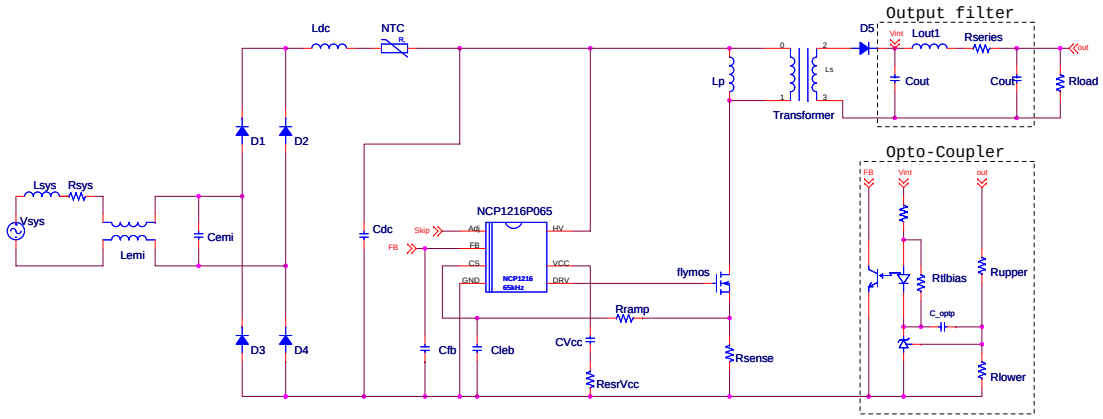


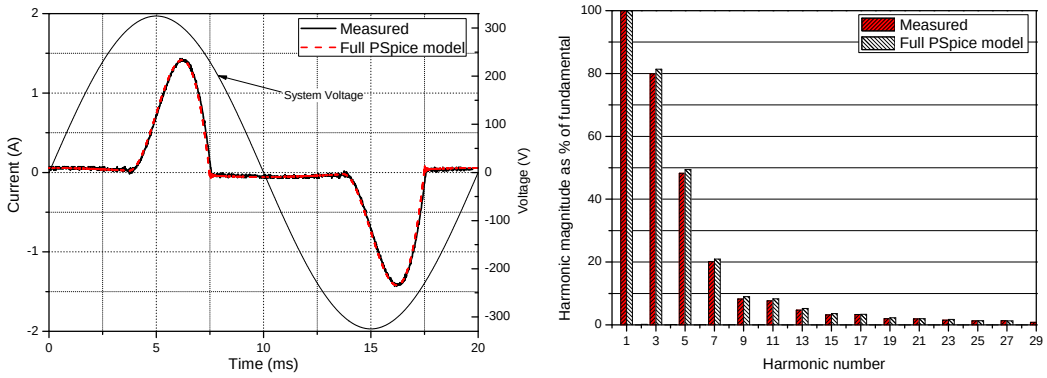
Figure 4.6: *Schematic of a full PSpice flyback-based SMPS model.*

4.3.2 Validation of full PSpice SMPS model

The developed PSpice SMPS model is validated in laboratory measurements. The SMPS power supply selected for measurement was from a desktop PC manufactured in 2004, with rated maximum power of 250W. The PC power supply was removed from the PC housing, and its output is loaded with a fixed resistive load of 100W. A fully controlled linear power supply, [90], was used to supply an ideal sinusoidal input voltage. The input current waveforms drawn by the PC power supply were measured, along with the input voltage for a voltage range of 0.8 to 1.2pu. The fixed resistive load was used, so that the output power drawn from the SMPS

could be maintained constant. This is hard to achieve if the power supply remains in the PC, as the power demand of the PC is constantly changing.

After completing the measurements, the PC power supply was disassembled and power supply components C_{dc}, C_{emi} and L_{dc} were identified and measured. It was further noted that PC power supply was of forward-converter topology. The measured component values were then applied to the full PSpice SMPS model. The dc-dc converter output voltage in the SMPS model was set to match that of the measured PC power supply, with the same value of load resistance applied. The topology of the SMPS model was left unaltered. Simulations were run for a range of system voltages between 0.8 to 1.2pu. Figures 4.7 and 4.8 show the comparison of measurements with the results from the PSpice SMPS model.



(a) Current/voltage waveforms

(b) Current harmonics

Figure 4.7: *Comparison between measured and full PSpice model of 250W SMPS.*

The results presented in Figure 4.7 show that the full PSpice SMPS model is able to very accurately predict the shape of the input instantaneous current waveform and its harmonics. Further results presented in Figure 4.8 show that, as expected, the active power demand characteristics of the SMPS are essentially constant with the steady-state changes in system supply voltage, and that PSpice model is also able to predict them accurately. The Q_1-V characteristics of the measured SMPS are nearly linear, showing that Q_1 reduces with the increase of input voltage. The PSpice model is also able to predict Q_1-V characteristics of the measured SMPS accurately, with a maximum error of $\pm 5\%$ (seen at the ends of the considered voltage range). The PF-V, PF_1-V, PF_d-V and THD-V characteristics of the measured SMPS can also be predicted by the PSpice model without any significant error.

The analysis presented in this section has shown that the full PSpice model of the SMPS is an accurate representation of an actual SMPS. Further, it has been shown that the topology of the dc-dc converter found within the SMPS will have no significant effect on the power characteristics of the SMPS.

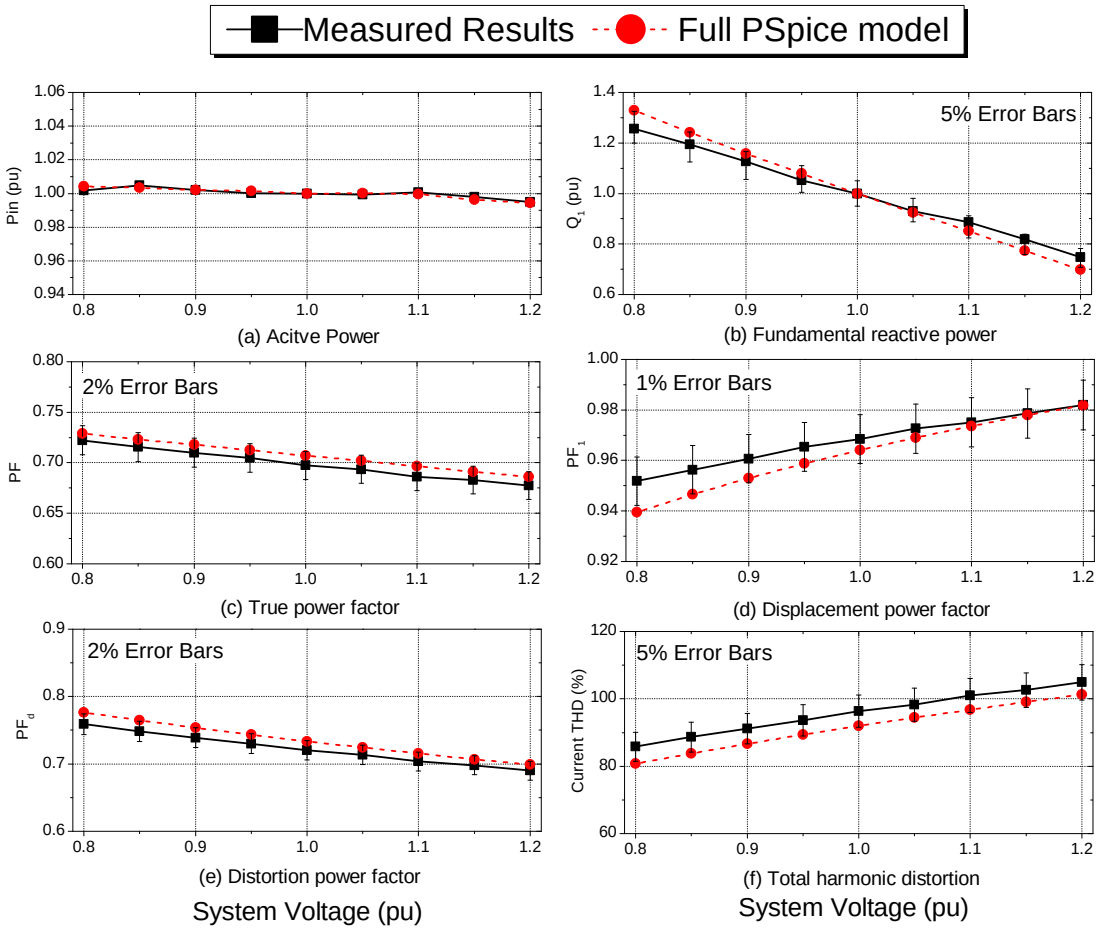


Figure 4.8: *Comparison of measurements with full PSpice SMPS model.*

4.4 Harmonic limits

Switch-mode power supplies connected to the EU supply network must comply with harmonic limits stipulated in [30], introduced in 2001. These standards state that SMPS' with rated power less than 75W are not subject to any harmonic limits. For SMPS' of rated power above 75W, used in e.g. personal computers, monitors or TVs (the overwhelming majority of SMPS' found at these power levels), [30] stipulates stringent harmonic limits (termed as Class D limits). There are two requirements stipulated by Class D, which are summarised in Table 4.2, both of which must be met in order for the SMPS to conform to this legislation. The first limit (Table 4.2, column 2), sets the maximum permissible harmonic current of a particular harmonic based on rated power of SMPS. The second limit (Table 4.2, column 3), sets an absolute maximum allowed harmonic current, and is not based on the rated power of the SMPS. These absolute limits are the same as the Class A limits considered in Section 3.6. These two sets of limits may be correlated to each other, as shown in Table 4.2, column 4, giving a maximum power above which harmonic limits in column 2 will breach limit in column 3.

Table 4.2: *EU harmonic emission standards, Class D limits [30].*

Harmonic order n	Maximum permissible harmonic current per watt (mA/W)	Maximum permissible harmonic current (A)	Correlating to maximum power of (W)
3	3.4	2.3	676
5	1.9	1.14	600
7	1.0	0.77	770
9	0.5	0.40	800
11	0.35	0.33	943
13	0.3	0.21	700
$13 \leq n \leq 39$	$\frac{3.85}{n}$	$0.15 \times \frac{15}{n}$	584

4.4.1 Methods of meeting harmonic limits

Manufacturers of SMPS' use either passive or active power factor correction (PFC) techniques to meet specified Class D harmonic limits. These active and passive PFC techniques are exactly the same as those used in SASD.

4.4.1.1 Active PFC

Active PFC is achieved by adding an additional dc-dc converter stage (besides that used for stabilising dc link voltage) to the SMPS. An SMPS with active power factor correction will draw constant active power from the supply system with changes in system voltage, and will draw essentially no fundamental reactive power, as discussed in Section 3.6.1.1. The active PFC controller will also adjust the input current waveform of the SMPS, making it to match the shape of the system voltage, i.e. it will not draw harmonic current (see Figure 4.10).

4.4.1.2 Passive PFC

Passive PFC is achieved by addition of a relatively large inductor, L_{dc}, to the rectifier circuit. This inductor will act to 'smooth' the rectifier input current pulse, as described in Section 3.3.1, therefore reducing its harmonic content. The full PSpice SMPS model developed in the previous section was used to investigate the expected value of L_{dc} in SMPS with passive PFC. The full model was adjusted to operate at rated powers between 75W and 500W. At each rated power, the absolute value of C_{dc} was set using the typical per-unit value of C_{dc} as found in Section 4.2.3. Simulations were then run with each of these models, and the value of L_{dc} was increased until Class D harmonic limits where just met. In this way, the minimum value of L_{dc} required to meet Class D harmonic limits was found as a function of SMPS rated power. The same analysis was also performed at values of C_{dc} 40% greater and 40% less than nominal, in order to quantify the effect of C_{dc} on L_{dc}. The results of this analysis are shown in Figure 4.9.

Also shown in this figure is the value of L_{dc} measured from the PC power supply used in the previous analysis.

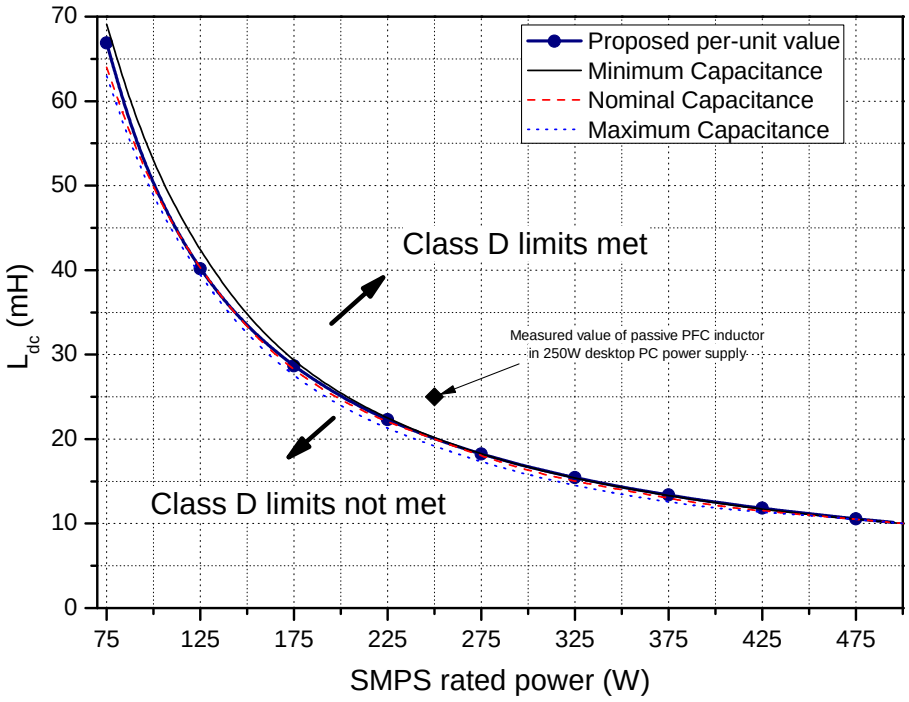


Figure 4.9: *Minimum size of L_{dc} required to meet Class D limits, [30].*

It can be seen from the results presented in Figure 4.9 that the value of C_{dc} only has a small effect on the selection of L_{dc}, as was the case with SASD load (see Section 3.6). It can also be seen that the relationship between L_{dc} and rated power of SMPS is continuous, and that the required value of L_{dc} will decrease as rated power of SMPS increases. This is in contrast to the results obtained for the SASD, where it was seen that relationship between rated power of SASD and value of L_{dc} was discontinuous, and that required L_{dc} increased with rated power of SASD. These differences are due to the harmonic limits applied to these two types of non-linear loads. The SMPS Class D harmonic limits are based on the rated power of the SMPS, while the SASD Class A (Table 4.2, column 3) limits are not.

As Class D harmonic limits are a function of SMPS rated power, a per-unit value of L_{dc} may be found, able to represent the value of this parameter over the whole considered power range of SMPS' with passive PFC. In order to find this per-unit value, any pair of SMPS rated power and L_{dc} values can be selected from Figure 4.9. As an illustration, a 250W SMPS is selected, for which associated L_{dc} is 20mH. This value is then converted to a per-unit reactance, by implementing (4.4), which gives $X_{Ldc} = 0.03$ pu.

$$X_{Ldc} = \frac{L_{dc} \cdot \omega}{\left(\frac{V_{phase}^2}{P_{SMPS}}\right)} = \frac{0.02 \cdot 2 \cdot pi \cdot 50}{\left(\frac{230^2}{250}\right)} \approx 0.03pu \tag{4.4}$$

Where: V_{phase} is the input phase voltage, P_{SMPS} is the rated power of the SMPS, $\omega = 2\pi f$ where f is the system frequency.

A plot of this proposed per-unit value of L_{dc} is also shown in Figure 4.9. It can be seen that the proposed per-unit value is indeed valid, as it closely follows values of L_{dc} obtained from harmonic legislation. This result is significant, as it means that the value of L_{dc} in the SMPS with passive PFC may be directly represented as a per-unit value without introducing an error. This was not the case for the SASD load, where it was not possible to derive such a general (i.e. unified) per-unit expression.

4.4.2 Categorisation of electronic dc power supply loads

The harmonic limits discussed above mean that the dc power supply load type should be subdivided into three following sub-types:

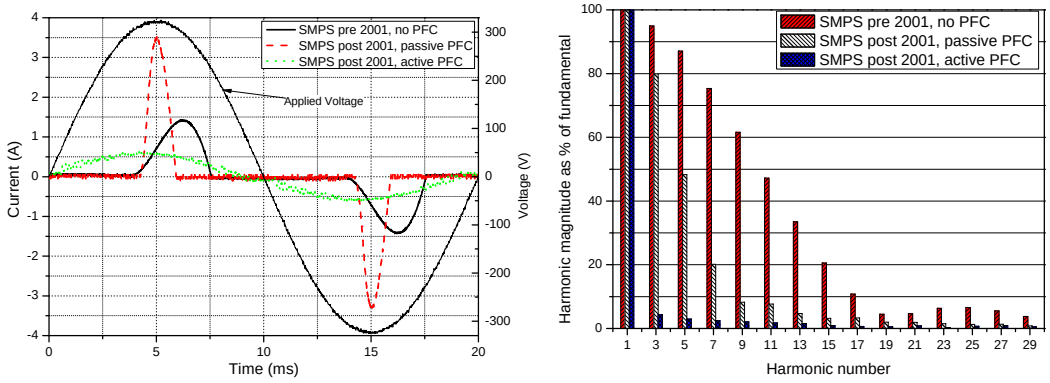
dc power supply with no PFC This load sub-type will be of rated power less than 75W, and will not include L_{dc} in the rectifier circuit.

dc power supply with passive PFC This load sub-type will be of rated power above 75W, and will have an inductor L_{dc} in the rectifier circuit ($X_{Ldc} = 0.03$pu).

dc power supply with active PFC This load sub-type will will be of rated power above 75W, and it will have an additional dc-dc converter stage to control the input current, making it sinusoidal and in-phase with the supply system voltage.

It is interesting to briefly compare the harmonic content of SMPS with and without PFC to show the effect of harmonic legislation (introduced in 2001) on the characteristics of the dc power supply load type.

The power supply from a PC manufactured in the year 2000 was removed from the PC and resistive load was applied to the dc output in the same way as described in Section 4.3.2. A sinusoidal voltage at 1 pu magnitude was applied to this pre-2001 SMPS and the input current waveform was measured. The same process was repeated for a PC power supplies manufactured post-2001 with active and passive PFC. Figure 4.10 shows a comparison between measured currents and associated harmonics of the pre-2001 and post-2001 SMPS'.



(a) Current waveforms (b) Harmonics

Figure 4.10: *Comparison between 250W PC power supplies with active and passive PFC (post-2001) and without PFC (pre-2001).*

The comparison of the three PC power supplies shown in Figure 4.10 highlights the effect of PFC on the wave shape and harmonic content of SMPS current. It can be seen that the 3^{rd} harmonic of the SMPS with passive and SMPS with no PFC are similar. However, higher order harmonics of the SMPS with passive PFC are considerably lower in magnitude than those of the SMPS without PFC. The current THD of the SMPS with no PFC is approximately 210%, compared to 80% of the SMPS with passive PFC which clearly express the difference in the harmonic content. It is also interesting to note that the displacement power factor (PF_1) of SMPS with no PFC is 0.995 "leading" compared to 0.97 "lagging" for the SMPS with passive PFC. Therefore, the effect of passive PFC is to increase SMPS true power factor ($PF_1 \cdot PF_d$), but decrease PF_1 and changing it from a "leading" to a "lagging" power factor. Hence, SMPS with passive PFC will draw fundamental reactive power and be inductive loads, while SMPS with no PFC will be a source of fundamental reactive power and act as capacitive loads (although only a small amount, as their $PF_1 \approx 1$). Therefore, the term "power factor correction" is somewhat misleading when considering SMPS with passive PFC. Active PFC, on the other hand will draw power with near unity values of both PF_1 and PF_d, as can be seen from the shape of its input current waveform in Figure 4.10.

4.5 Development of equivalent circuit and analytical dc power supply models

As in case of ASD and SASD loads, an analytical model of the dc power supply, i.e.SMPS, is developed and validated in this section. Each of the main SMPS component blocks are now discussed and converted to equivalent circuit and then into analytical form.

4.5.1 EMI filter

As discussed previously, the EMI filter circuit shown in Figure 4.3 will consist of a common-mode choke, L_{emi}, and capacitor, C_{emi}. The common-mode choke has no effect on the operation of the SMPS from a load modelling point of view, as it will only present impedance to unbalanced currents, causing high frequency noise. However, as can be seen from Figure 4.3, C_{emi} is connected in parallel with the supply system, and some shunt current can flow. The magnitude of this current will be small, as C_{emi} is of a low value, in the order of nF. The effect of C_{emi} has already been shown in Figure 4.7(a), where a small continuous ac current component can be seen between the current pulses. This component is not represented in the developed analytical models, as it will not have any significant effect on power demand characteristics of the SMPS.

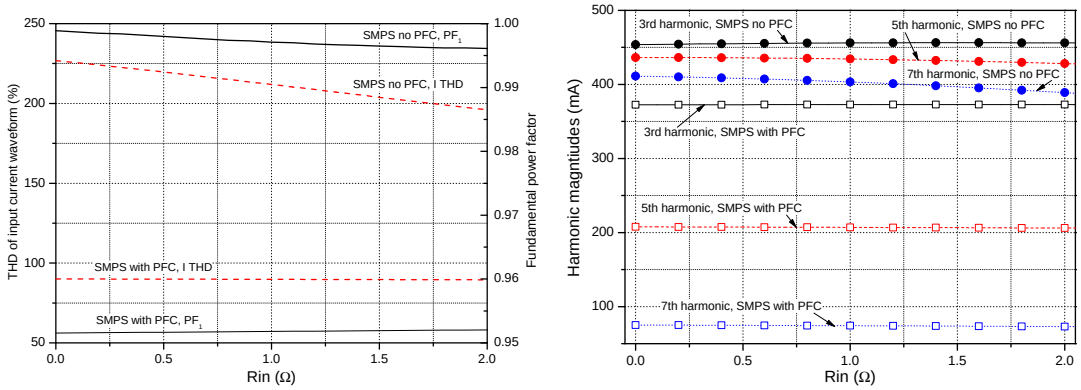
4.5.2 NTC Thermistor

The NTC thermistor will have the greatest effect on the SMPS with no PFC, as it will account for a significant part of the bridge rectifier conduction path impedance. The NTC thermistor is expected to have a much smaller effect on SMPS with passive PFC, as L_{dc} will dominate the rectifier conduction path impedance. In order to quantify the effect of the thermistor, the full PSpice SMPS model was set-up to model a 75W SMPS with and without passive PFC. The reactance of C_{dc} in both models was taken as 0.036pu, and the reactance of L_{dc} in the SMPS with passive PFC taken as 0.03pu (i.e. nominal values of C_{dc} and L_{dc}).

The expected value of thermistor resistance is approximately $1-2\Omega$ for the thermistor operating in (thermal) steady state, (i.e. "hot resistance"). This is because "hot resistance" values greater than 2.0Ω will cause excessive losses in the bridge, while "hot resistance" lower than 1.0Ω are unlikely to increase enough when thermistor is "cold" to provide effective inrush current protection. Simulations were run on both models with the thermistor replaced by a resistor. The value of this resistor was changed between 0.0Ω and 2Ω. The results of this analysis are shown in Figure 4.11.

The results presented in Figure 4.11(a) clearly show that the size of R_{in} (i.e. the thermistor resistance) has no significant effect on the THD or the displacement power factor of the SMPS with passive PFC. This also applies to harmonics, where the 3^{rd}, 5^{th} and 7^{th} harmonics of the SMPS input current waveform are unchanged by the value of R_{in}. Thus, when developing the analytical model of the SMPS with passive PFC, the thermistor does not need to be considered.

The THD of the SMPS without PFC will be affected by additional resistance in the bridge rectifier, as illustrated in Figure 4.11(a). The same is true for the displacement power factor, which will decrease for larger values of R_{in}. The 3^{rd} and 5^{th} harmonics of this type of SMPS



(a) THD and PF_1

(b) 3^{rd}, 5^{th} and 7^{th} harmonics

Figure 4.11: *Effect of thermistor resistance on characteristics of SMPS with and without passive PFC.*

are relatively unaffected by change in R_{in}, although the magnitude of the 7^{th} harmonic will decrease slightly with increasing values of R_{in}. Therefore, the thermistor should be represented in simplified analytical models of the SMPS with no PFC. This completes the analysis of the front-end components of an SMPS.

4.5.3 Equivalent circuit and analytical model of dc power supply load

In previous chapters, the equivalent circuit models of considered non-linear load types (ASD and SASD) have taken the form of a front-end rectifier with applied equivalent resistive load. These equivalent resistive loads have been determined to produce the correct P-V characteristics of the modelled loads. Previous work on equivalent/analytical representation of SMPS has followed a similar approach, e.g. [91] and [79], although SMPS P-V and N-V power demand characteristics are not considered there. Thus, if the SMPS dc-dc converter and the load it supplies are represented as an equivalent resistance, the equivalent circuit shown in Figure 4.12 may be used to simplify the model of the SMPS.

From the discussions and the results presented in the preceding sections, it has been shown that the SMPS will draw effectively constant active power from the supply system, independently of changes in supply system voltage. Therefore, the equivalent resistance in Figure 4.12 may be represented as a function of the rated power of the SMPS and the rectifier dc link voltage:

$$R_{eq} = \frac{v_{dc}^2}{P_{SMPS}} \tag{4.5}$$

Where: R_{eq} is the equivalent resistance, v_{dc} is the instantaneous rectifier dc link voltage and P_{SMPS} is power supplied by the rectifier to the dc-dc converter, i.e rated power of SMPS (as

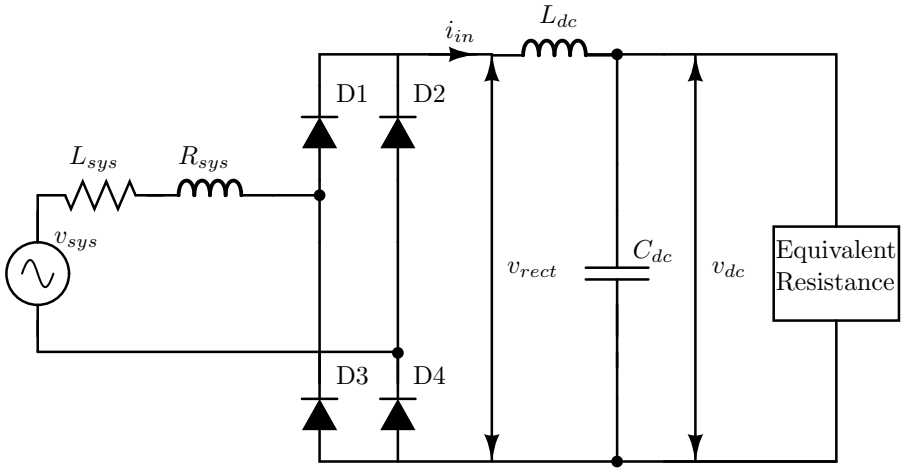


Figure 4.12: *Equivalent circuit model of SMPS.*

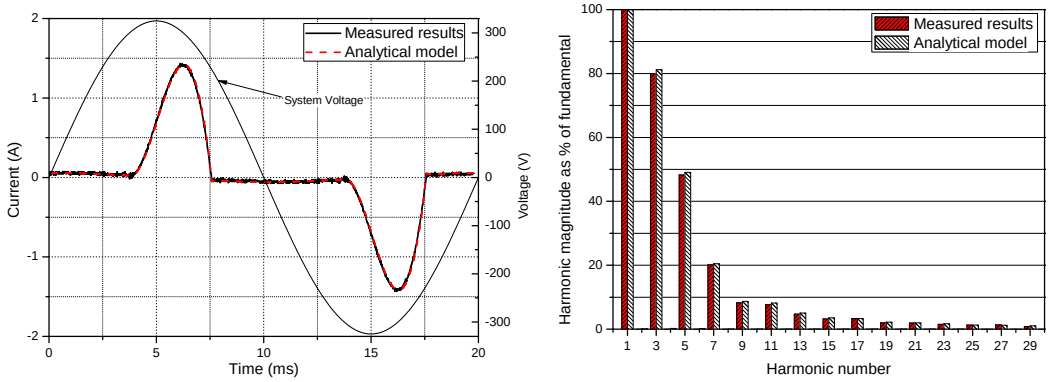
rectifier losses are low).

The analytical model of the equivalent circuit shown in Figure 4.12 has already been developed and validated in Section 3.10 and therefore this discussion will not be repeated here. This previously developed analytical model may be used directly for the representation of the SMPS load, if the equivalent resistance is substituted with expression (4.5).

4.6 Validation of equivalent circuit and analytical models of dc power supply load

The proposed equivalent circuit and analytical models of the SMPS are validated in this section using measured data. It is assumed that validation of the analytical model also validates the equivalent circuit model. As in the preceding chapters, the model is supplied with both ideally sinusoidal and distorted (non-sinusoidal) voltages to confirm its ability to represent SMPS load in both situations. Two non-sinusoidal voltage waveforms are used: "typically distorted" and "heavily distorted" as in Section 2.12.2. The measured SMPS was the 250W PC power supply (with passive PFC) used previously to validate the full PSpice SMPS model. The component values, C_{dc} and L_{dc} of this dc power supply were measured and applied to the analytical model and P_{load} in expression 4.5 set to 100W. Figures 4.13, 4.15 and 4.17 show the input current waveforms and associated harmonics of the analytical model compared with the measured results for applied sinusoidal, "typically" and "heavily" distorted supply voltage with magnitude of 1pu. Figures 4.14, 4.16 and 4.18 show comparisons of P-V and N-V power demand characteristics between the measured and modelled SMPS, again for applied sinusoidal, "typically" and "heavily" distorted supply voltage.

4.6.1 Sinusoidal supply conditions



(a) Current/voltage waveforms (b) Current harmonics

Figure 4.13: *Comparison between measured results and analytical model of 250W SMPS, with applied sinusoidal system voltage.*

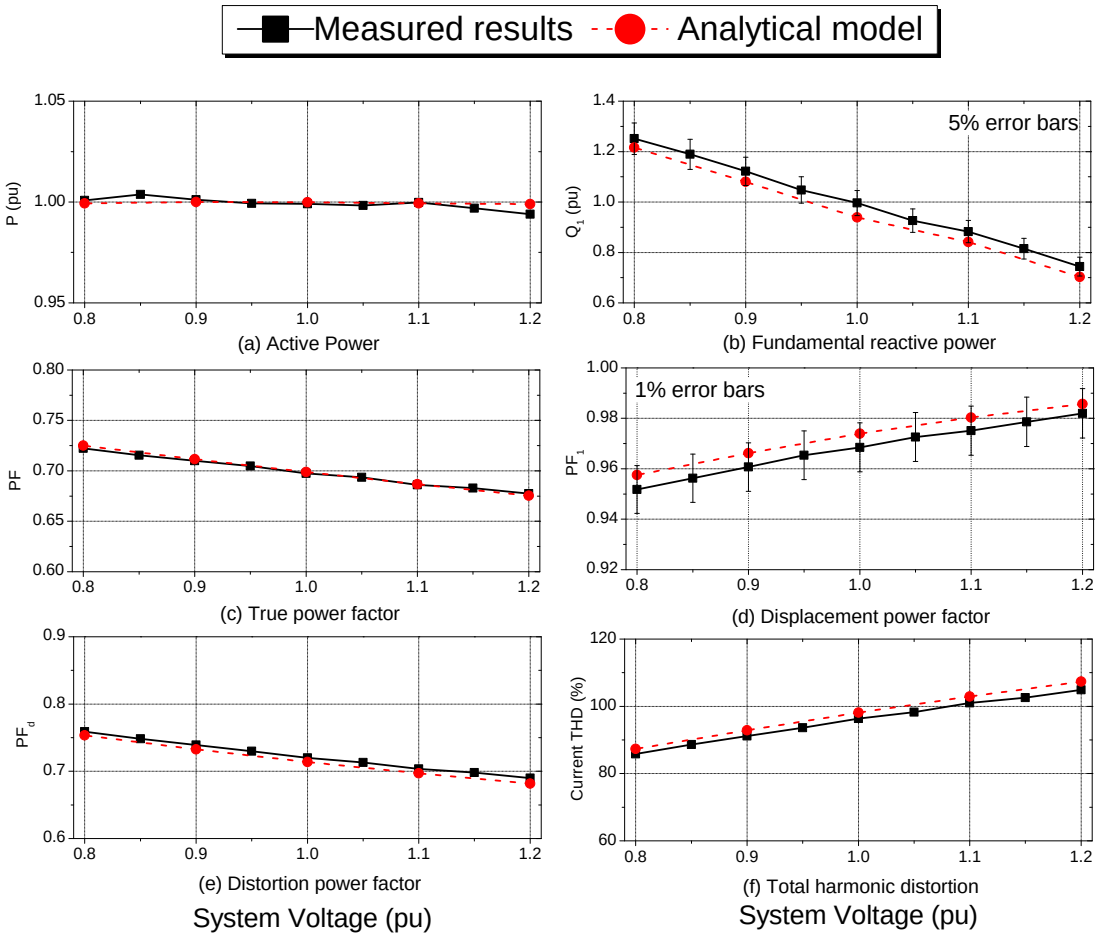
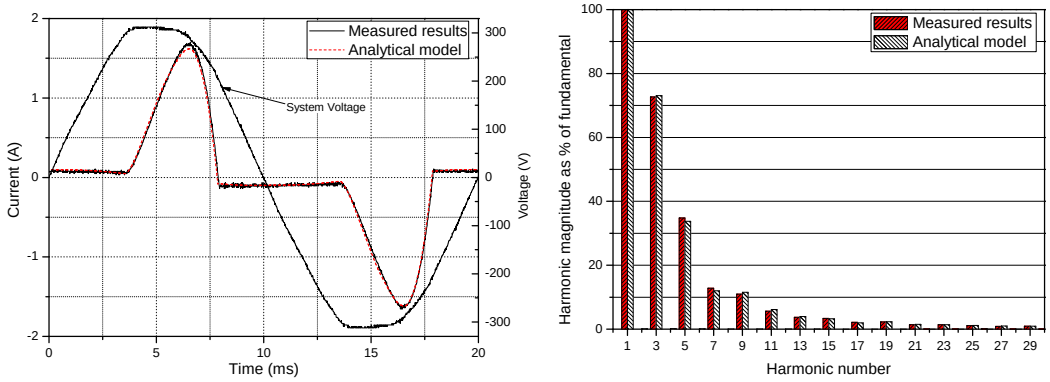


Figure 4.14: *Comparison of power demand characteristics between measured 250W SMPS and analytical model of 250W SMPS with passive PFC for sinusoidal supply voltage.*

4.6.2 Non-sinusoidal supply conditions



(a) Current/voltage waveforms (b) Current harmonics

Figure 4.15: *Comparison between measured results and analytical model of 250W SMPS, with applied "typically distorted" system voltage.*

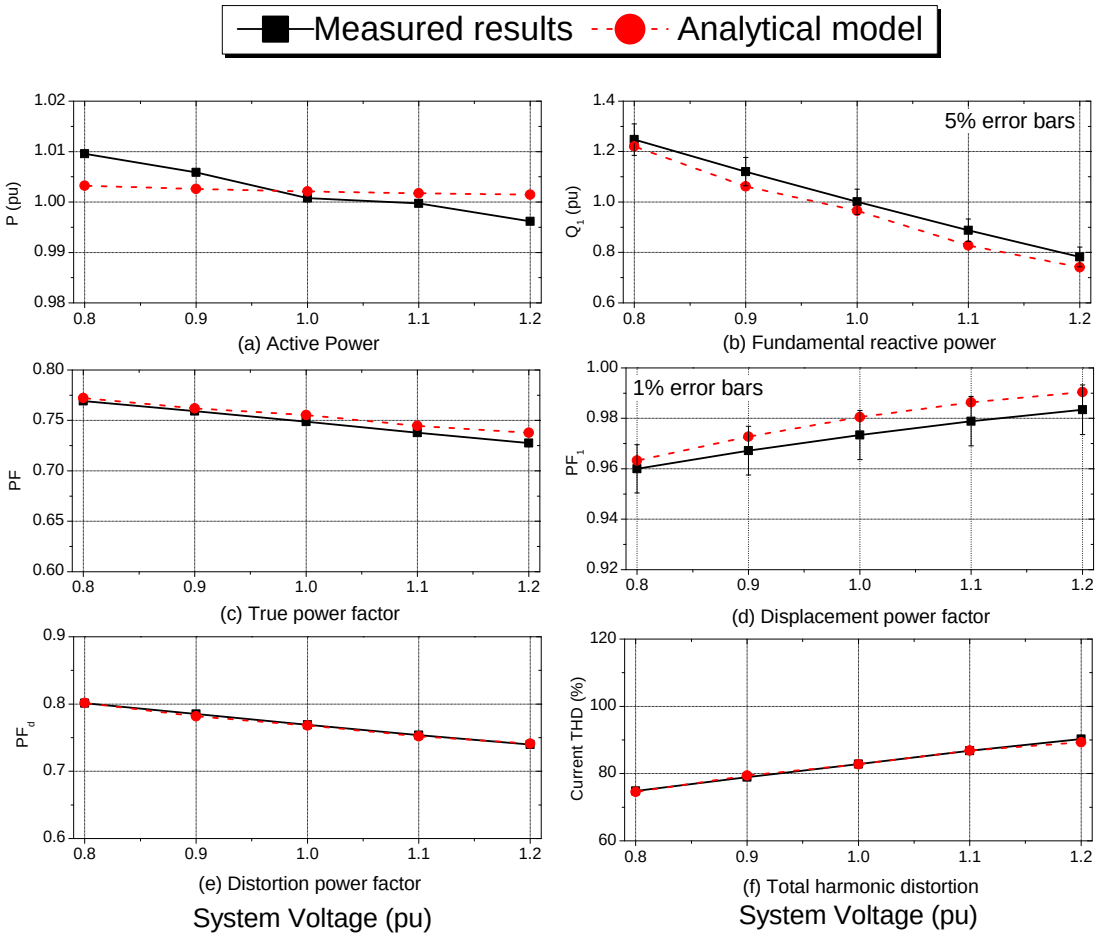
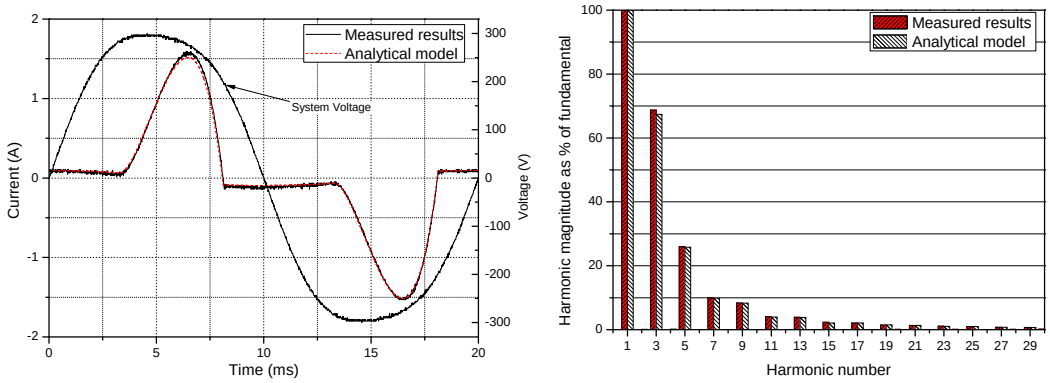


Figure 4.16: *Comparison of power demand characteristics between measured 250W SMPS and analytical model of 250W SMPS with passive PFC for "typically distorted" supply voltage.*



(a) Current/voltage waveforms (b) Current harmonics

Figure 4.17: *Comparison between measured results and analytical model of 250W SMPS, with applied "heavily distorted" system voltage.*

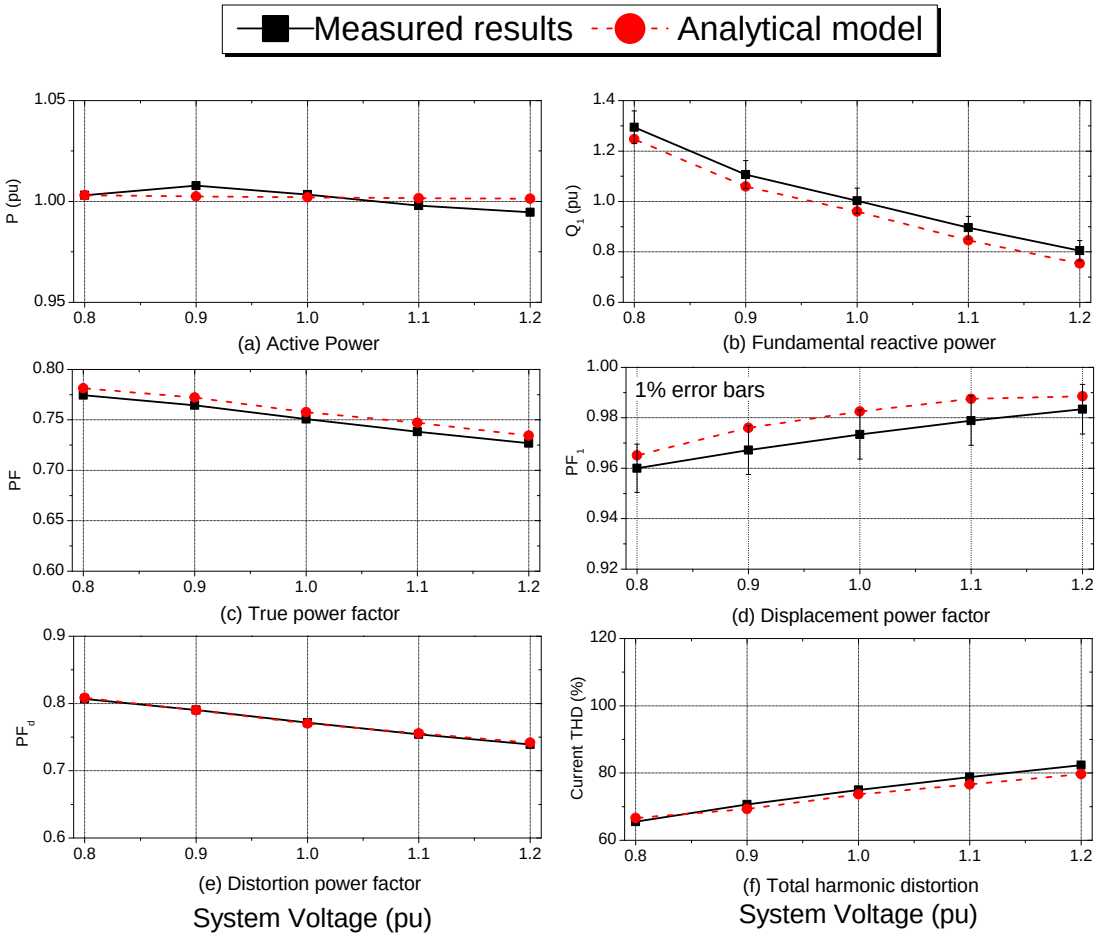


Figure 4.18: *Comparison of power demand characteristics between measured 250W SMPS and analytical model of 250W SMPS with passive PFC for "heavily distorted" supply voltage.*

4.6.3 Discussion of results

The P-V characteristics of the measured SMPS are essentially constant, showing no more than a 1% deviation from the nominal value of active power for all applied (including non-sinusoidal) voltage supply conditions. Therefore, these P-V characteristics can be easily represented by the constant active power analytical model.

The comparison of Q_1-V characteristics between the analytical model and measured values are also in good agreement to each other, with no more than 5% error. It can also be seen from Figures 4.14, 4.16 and 4.18 that shapes of the Q_1-V characteristics predicted by the analytical model are almost identical to that of the measured results. However, at 1pu system voltage the values of Q_1 do not exactly match, which is the main reason for the small observed error. This error is due to a difference of less than 1% in predicted and measured values of PF_1, and is deemed to be within acceptable limits.

The PF-V, PF_d-V and THD-V characteristics of the analytical model also very closely match those of the measured SMPS for all applied (sinusoidal and distorted) voltages. This shows that a good matching of current waveforms and harmonics in Figures 4.13, 4.15 and 4.17 is preserved for system voltage magnitudes other than 1pu.

It can be seen that distortion of the system voltage will reduce the harmonic content of the current drawn by the SMPS with passive PFC, which was also the case for higher-power SASD load. Figures 4.13, 4.15 and 4.17 show that the THD of the current waveform of considered SMPS is approximately 98% for 1pu voltage under ideally sinusoidal supply conditions. This reduces to 75% for "heavily distorted" 1pu supply conditions. It can as well be seen from these figures that the first few harmonics are responsible for these changes of the THD, as their magnitudes are significantly greater than those of the higher order harmonics. Furthermore, like the higher-power SASD load, the displacement power factor of the SMPS with passive PFC is not significantly affected by distortion in the supply system voltage.

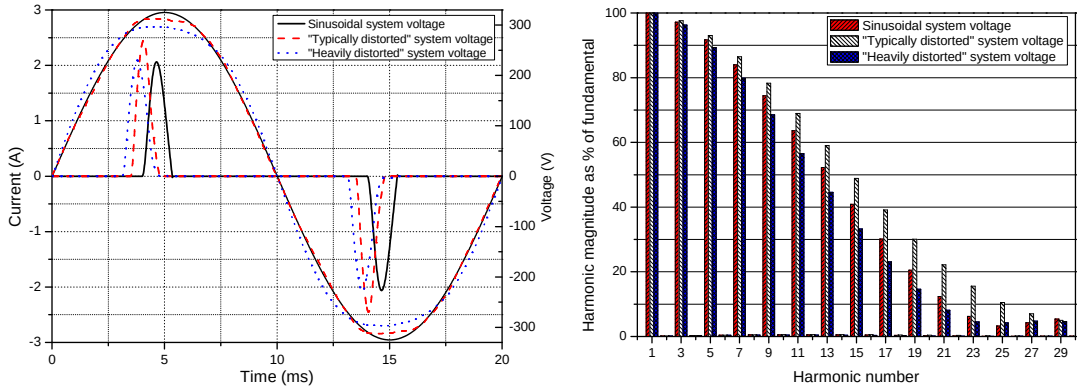
The effect of change in supply system impedance has not been specifically considered, as it will have essentially no effect on the P-V or N-V power demand characteristics of the SMPS with passive PFC, due to a significant inductance in bridge rectifier conduction path, L_{dc}.

From the presented results, it can be concluded that the analytical model of the SMPS is able to accurately represent both harmonic and power demand characteristics of an actual (and measured) SMPS for both sinusoidal and non-sinusoidal supply conditions.

4.7 Characteristics of SMPS with no PFC

The characteristics of the SMPS with no PFC are now briefly considered, as they have not been specifically discussed previously. The analytical model of SMPS has been verified in the previous section and therefore it is used for this investigation. The analytical model was set to represent an SMPS of rated power 50W, with value of C_{dc} found from typical per-unit value, R_{in} set to 1.5Ω and L_{dc} set to zero. The value of system impedance was first altered between minimum and maximum values (see Section 1.8) for applied sinusoidal conditions, in order to quantify the effects of system impedance on the SMPS. Then, system impedance was set to nominal and "typically" and "heavily" distorted system voltages applied. For each of the considered cases system voltage was varied between 0.8-1.2pu, in order to obtain the SMPS' P-V and N-V power demand characteristics.

Figure 4.19 shows the input current waveforms and associated harmonics of the SMPS with no PFC for applied 1pu sinusoidal supply system voltage, as well as for "typically" and "heavily" distorted system voltages. Figure 4.20 shows the P-V and N-V power demand characteristics for each considered case. The results for P-V and Q_1-V power demand characteristics are presented in per-unit, for which base values are taken as the absolute values of P or Q_1 at 1pu system voltage. In this way, the differences or similarities in shapes of the characteristics, specifically the Q_1-V power demand characteristics, may be better seen.



(a) Current/voltage waveforms

(b) Current harmonics

Figure 4.19: *Input current waveforms and associated harmonics of SMPS with no PFC for applied, sinusoidal, "typically distorted" and "heavily distorted" system voltages.*

The results of this analysis are very similar to the results presented previously for lower-power SASD load (see Section 3.12.2) and so are only briefly discussed here. The P-V power demand characteristics are once again invariant to changes in system impedance and supply voltage distortion. It can be seen that under sinusoidal conditions the SMPS with passive PFC will operate with close to unity displacement power factor and that variation in system impedance will not have any significant effect on displacement power factor. Therefore, for

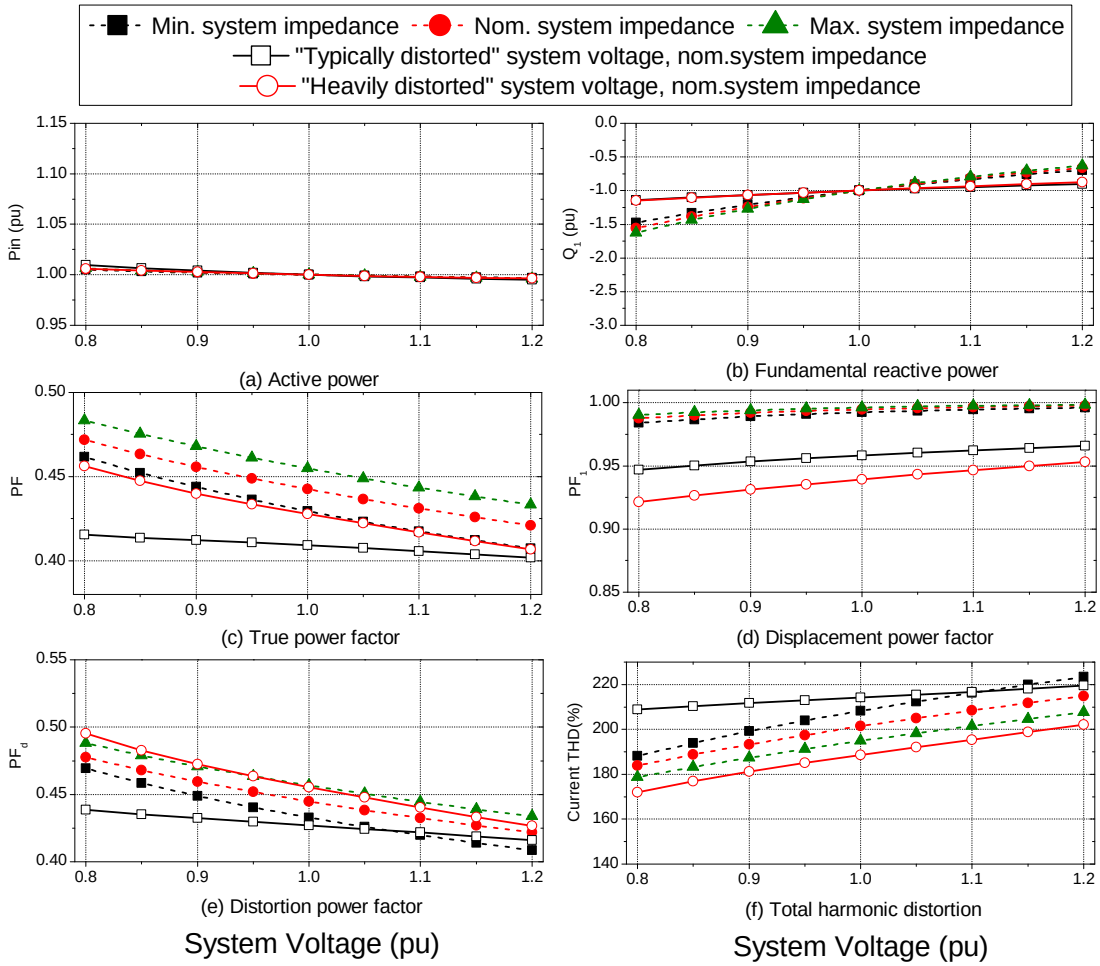


Figure 4.20: *P-V and N-V power demand characteristics of SMPS with no PFC for minimum, nominal and maximum values of system impedance and sinusoidal system voltage, and for nominal system impedance and applied "typically distorted" and "heavily distorted" system voltages.*

SMPS supplied with ideal sinusoidal voltage,Q_1-V power demand characteristics are not of particular importance, as Q_1 will be essentially zero (PF_1 close to unity). However, when supply system voltage becomes distorted, displacement power factor of the SMPS with no PFC reduces significantly, as was the case in lower-power SASD load. For this situation the Q_1-V power demand characteristics of the considered SMPS are close to constant current characteristic. As well, this load is capacitive, and becomes increasingly capacitive the more distorted the system becomes.

The current THD of the SMPS with no PFC will be affected by both change in supply system impedance and distortion in the system voltage, and the reasons for this have been previously considered in Section 3.12.2. It should be noted that the SMPS with no PFC will draw more distorted current than lower-power SASDs, because SMPS' will have larger values of C_{dc} (X_{Cdc} in the SMPS with no PFC is 0.036, compared to 0.075 in the SASD).

4.8 Generic analytical models of dc power supply loads

The developed analytical SMPS model is now used to form generic models of two of the three identified types of SMPS loads: the SMPS with no PFC, and the SMPS with passive PFC . The SMPS with active PFC requires no generic analytical model, as it may be presented as a linear load that draws constant active power with changes in system voltage. As discussed previously, generic analytical expressions of individual load types are needed, as it is not practical to aggregate a hundreds or thousands of individual load instances. Thus, generic analytical models may be used to represent the expected aggregate characteristics of a same type or sub-type load, allowing further aggregation with other load models in larger aggregate load mixes. In order to develop these generic analytical models, the analytical model parameters, R_{in}, C_{dc} and, where relevant, L_{dc} must be expressed in a per-unit form for the SMPS' with and without passive PFC. The development and validation of each generic model with measurements is now presented.

4.8.1 Generic model of SMPS without PFC

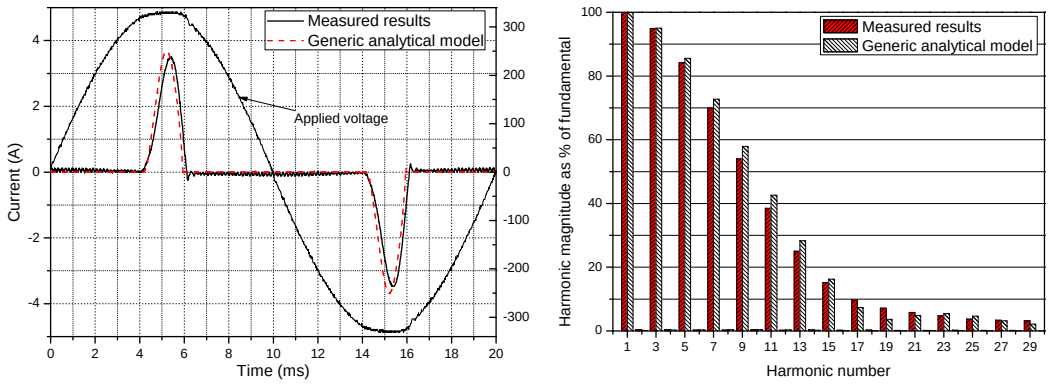
This sub-type of SMPS load will be of rated active power less than 75W, for which typical examples include laptop pc power supplies, CD/DVD players, small TVs, HiFi, etc. These loads will not have to conform to Class D limits, and hence will not contain any form of power factor correction. Therefore, the value of model parameter L_{dc} can be set to be zero. The nominal expected value of C_{dc} in the generic analytical model is taken as the per-unit value derived in Section 4.2.3. This leaves only the value of R_{in} to be defined which is considered below.

4.8.1.1 Per-unit value of R_{in}

A correct per-unit value of R_{in}, which is dominated by the steady-state resistance of the NTC thermistor, must be selected. In order for this per-unit value to be found, an assumption must be made as to the typical value of R_{in} at a particular rated power of SMPS. As discussed previously in Section 4.5.2, the value of R_{in} representing the NTC thermistor steady state resistance is very likely to be between $1 - 2\Omega$ for SMPS' of rated power up to 75W. The absolute value of R_{in} is taken as 1.5Ω for an SMPS of 50W rated power, which is selected here as a typical SMPS without PFC. Corresponding per-unit value of R_{in} in the generic model of SMPS with no PFC is 0.0014pu (for 50W base power and base impedance of $R_{base} = \frac{230^2}{50} \approx 1070\Omega$).

4.8.2 Verification of generic model of SMPS without PFC

The proposed generic analytical model of SMPS without PFC should be able to represent an aggregation of individual SMPS of the same sub-type. In order to validate this model, three 17" LCD computer monitors were connected to a controllable voltage source, [92], to form an aggregate SMPS load. The selected monitors were manufactured in 2007 and are accordingly representative of modern loads. Each monitor had rated power 45W, and the aggregate of the three drew 120W at nominal supply voltage. The monitors were set to display a screen of text, and the controllable voltage source is used to vary the supplied voltage between 0.8 and 1.2pu, so that the P-V and Q_1-V power demand characteristics of this aggregate load could be obtained. The generic analytical model of SMPS without PFC was set-up to represent this aggregate load, i.e. P_{load}, from (4.5), was set to 120W. The value of the controllable voltage source impedance was not exactly known, and there was no equipment available to measure this value. Therefore, an expected reasonable value was assumed. This value of system impedance was converted to per-unit, using the same base as for R_{in} (Section 4.8.1.1) and applied to the generic analytical model. The controllable voltage source was set to supply sinusoidal voltage to the aggregate load, but the harmonic content of this load was such that its output voltage became distorted. In order to provide a fair comparison between measurements and model, the distorted voltage was measured and reproduced in MatLab and supplied to the generic analytical model. Figure 4.21 shows the current waveforms and associated harmonics of measured aggregate load and the corresponding generic analytical model, while Figure 4.22 compares their P-V and N-V power demand characteristics.



(a) Current/voltage waveforms

(b) Current harmonics

Figure 4.21: *Comparison between measured aggregate load formed from three LCD monitors and corresponding generic analytical model of SMPS with no PFC, at 1pu system voltage.*

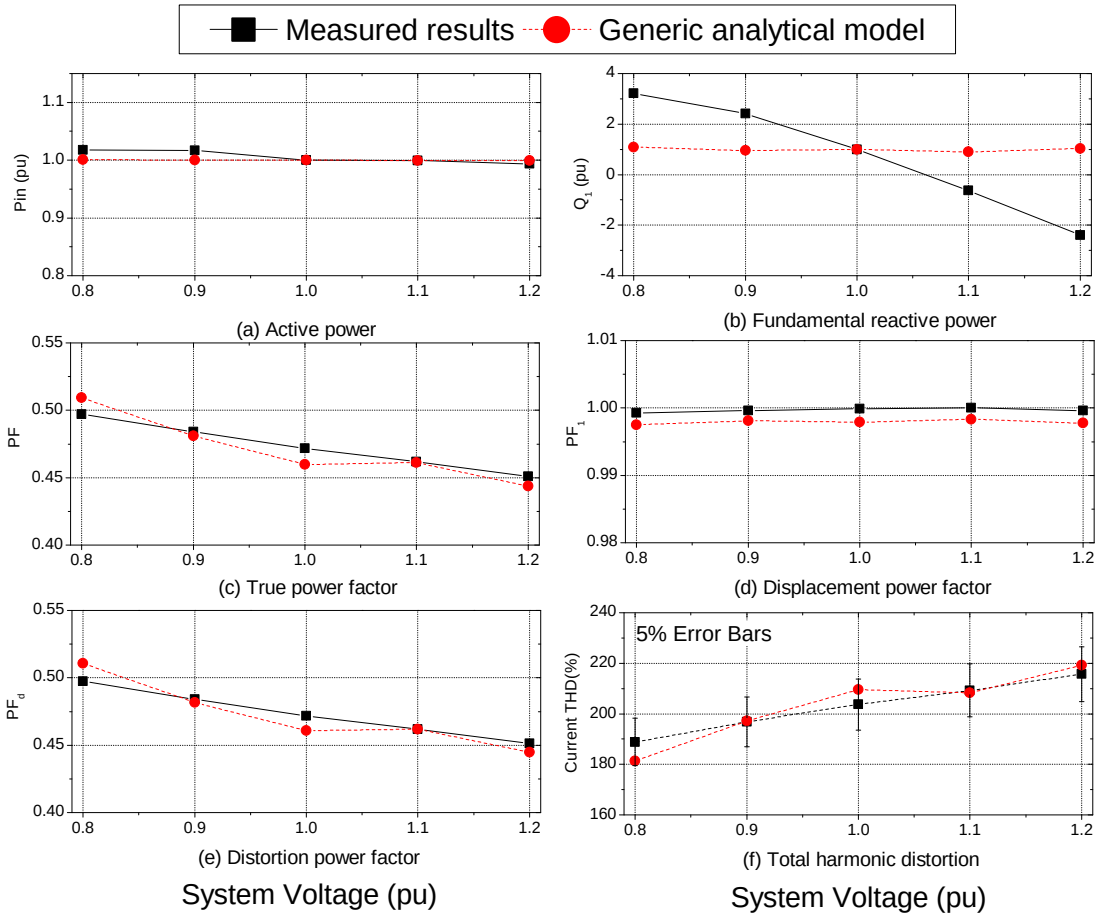


Figure 4.22: *Comparison of power demand characteristics between measured aggregate load formed from three LCD monitors and corresponding generic analytical model of SMPS with no PFC.*

The results in Figure 4.21 show that the generic analytical model is able to accurately predict the shape of the aggregate load input current and, accordingly, its harmonic content. The results also show that the monitors' P-V characteristics are essentially constant, and that the aggregate model can predict them with no significant error. The Q_1-V power demand characteristics of the aggregate load is, at first glance, strange, but it should be noted that measured displacement power factor of the load is 0.9997, and therefore this characteristic is not relevant as actual value of $Q_1 \approx 0$. All other power characteristics show close matching between measurements and proposed generic model.

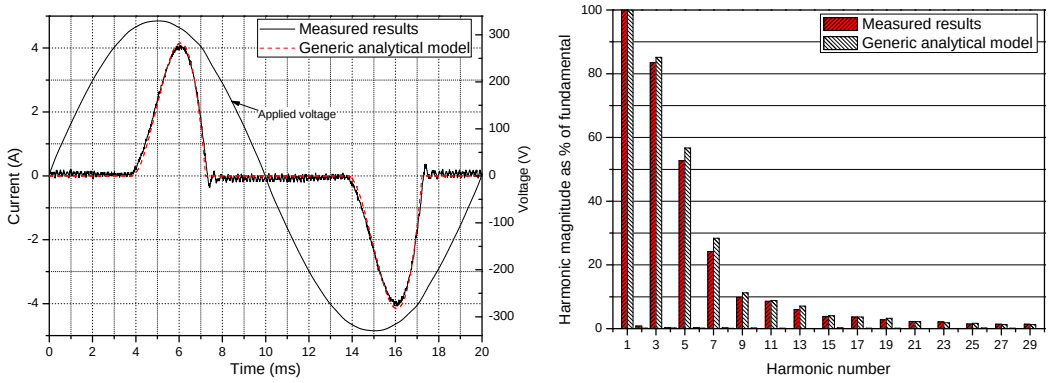
Therefore, these results show that the proposed generic analytical model of SMPS with no PFC may be used to represent an aggregate of this load sub-type. This result also further confirms that the per-unit value selected for C_{dc} is indeed valid, and that the assumption made for the value of R_{in} does not lead to significant error.

4.8.3 Generic analytical model of SMPS with passive PFC

The generic analytical model of SMPS with passive PFC can be developed in the same way as the generic model of the SMPS with no PFC. The per-unit value of C_{dc} in both models is the same. The value of the thermistor resistance, R_{in}, will have an insignificant effect on the characteristics of the SMPS with passive PFC, and so can be ignored, (see Section 4.5.2). Finally, the typical per-unit value of the parameter L_{dc} has already been defined, (Section 4.4.1.2) and this value can be used directly.

4.8.4 Verification of generic analytical model of SMPS with passive PFC

The proposed generic analytical model of the SMPS with passive PFC is validated in exactly the same way as the generic analytical model of the SMPS with no PFC in the previous section. However, this time the aggregate load consists of three PC's manufactured in 2007. Using PC load presents an additional problem, which was not apparent for monitors. The problem is that a PC will seldom operate at a constant power level. This is because at any time a PC may be performing a number of different tasks that demand different amounts of power from the dc power supply. It has already been shown previously that a PC power supply will have a constant P-V power demand characteristics if it supplies a constant dc load resistance. Therefore, P-V power demand characteristics of the aggregate load are not of interest in these comparison. The aim of this analysis is to validate that the generic analytical model can predict N-V characteristics of the considered aggregate PC load of given active power demand. Therefore, the generic analytical model was set to the specific power demand of the PC aggregate load at each considered voltage, so that the mentioned variations in P-V during normal operation do not influence the results for N-V comparisons. This method was used as there were no available post-2001 power supplies, that could be opened and resistive loads attached. The PCs were all set to play streaming media content during the measurements, so that they would draw fairly significant power. Each PC was rated for 250W, and the aggregate load of three PCs was measured at around 255W. The generic analytical model of the SMPS with passive PFC was set-up to model this load. Figure 4.23 shows the current waveforms and associated harmonics of measured aggregate load and the corresponding analytical model, while Figure 4.24 compares their P-V and N-V characteristics.



(a) Current/voltage waveforms (b) Current harmonics

Figure 4.23: *Comparison between measured aggregate load formed from three PCs and corresponding generic analytical model of SMPS with passive PFC, at 1pu system voltage.*

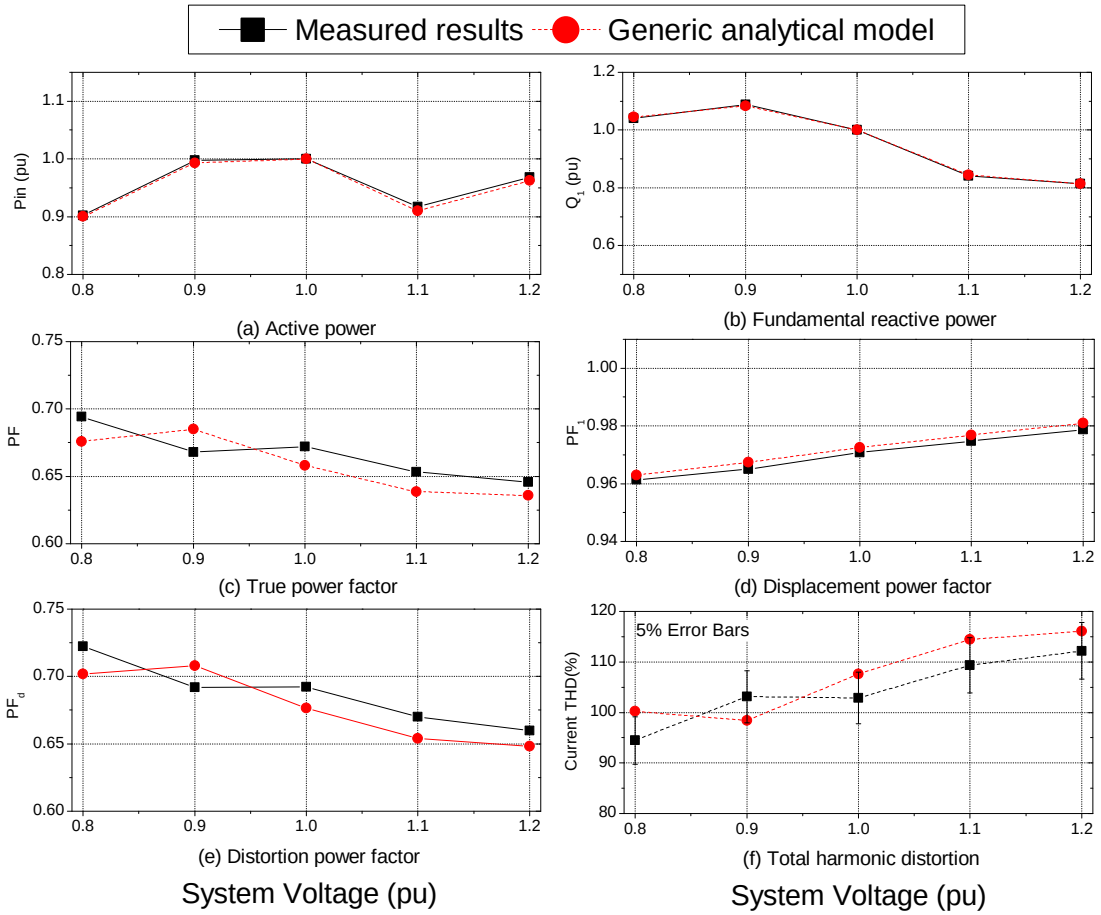


Figure 4.24: *Comparison of power demand characteristics between measured aggregate load formed from three PCs and corresponding generic analytical model of SMPS with passive PFC.*

The presented results show excellent matching of generic analytical model and measured

results. It can be seen from Figure 4.23 that the current waveform of the measured aggregate load is almost identical to that of the proposed generic analytical model. It can further be seen from results in Figure 4.24 that this matching will be also be maintained for other than nominal value of system voltage. The good matching of the model to measurements validates the per-unit value derived for L_{dc}, and other components from previous discussions. The results show that the proposed generic analytical model may be used to represent an aggregate load of this sub-type.

4.9 Polynomial and exponential models of dc power supply loads

The developed generic analytical SMPS models may now be used to derive polynomial and exponential models of these loads. As previously, the least square fitting method described in Section 2.7.1 is applied to the P-V and Q_1-V characteristics of the SMPS' without PFC and SMPS' with passive PFC to find the associated polynomial and exponential model coefficients. These coefficients are shown in Table 4.3, where the polynomial and exponential models of the SMPS' with active PFC are also presented. SMPS' with active PFC, as discussed previously, may be simply represented as constant active power linear loads.

Table 4.3: *Proposed, exponential and polynomial model coefficients of dc power supplies.*

PF_1	Exp. Model		Polynomial Model					
	np	nq	Z_p	I_p	P_p	Z_q	I_q	P_q
SMPS with no PFC								
0.994	0	2.36	0.00	0.00	1.00	-3.63	9.88	-7.25
SMPS with passive PFC								
0.970	0	-0.5	0.00	0.00	1.00	0.45	-1.44	1.99
SMPS with active PFC								
1.00	0	na	0.00	0.00	1.00	0	0	0

It can be seen from the results in Figure 4.25 that both polynomial and exponential models are able to accurately represent the characteristics of the two considered dc power supply load sub-types. Also shown in Figure 4.25 are plots of previously presented exponential and polynomial models of dc power supply loads, Table 4.1. It can be seen that models proposed in this thesis differ from existing models. The biggest difference can be seen between the previously presented exponential models of television load, [15]. From the discussions and measurements presented in this chapter, it is clear that this load model is now outdated. Modern televisions will have constant active power characteristics, while fundamental reactive power characteristics and power factor will be dependent on whether PFC is used in the television, and if so, on the type of applied PFC. The existing models of office equipment, [22], are also in

disagreement with the results presented in this chapter, which demonstrate that dc power supply loads are constant active power loads. Existing models of office equipment also state that the displacement power factor of this equipment is unity, and therefore they will draw no reactive power (no Q_1 values in Figure 4.25(b) and (d)). These models where developed in 1998, and therefore are likely be related to SMPS with no PFC, which explains this power factor. A large percentage of modern office equipment will consist of desktop PCs, which have been shown in this chapter to operate with displacement power factors less than unity (≈ 0.97). Finally, it has been shown that system voltage distortion will cause both Q_1-V and displacement power factor of SMPS with no PFC to change considerably, which none of the polynomial and exponential models (proposed and previous) can take into account.

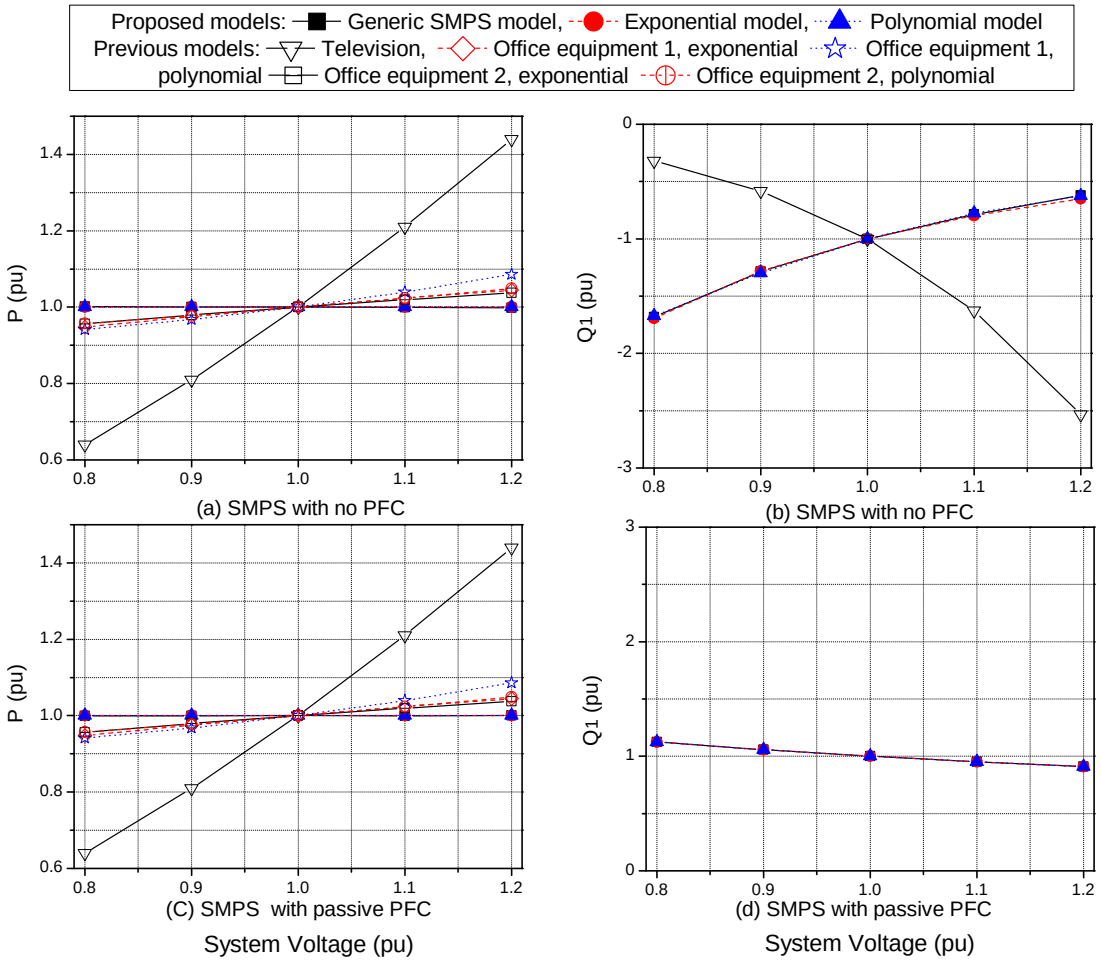


Figure 4.25: *Polynomial and exponential fits of P-V and Q_1-V characteristics of SMPS no PFC and with passive PFC.*

4.10 Conclusions

It has been shown in this chapter that harmonic legislation introduced in 2001 had significant effect on the non-active power demand and harmonic characteristics of the SMPS load type. This legislation led to creation of three distinct sub-types of SMPS load, defined as: SMPS with active PFC, SMPS with passive PFC and SMPS with no PFC. The SMPS with no PFC is of the same type as pre-2001 SMPS, when there was no harmonic legislation. Previous research into load modelling and harmonic characterisation of these loads has focussed on the SMPS with no PFC, as much of this work has been performed prior to 2001. The SMPS with passive PFC will have lower displacement power factor and will be an inductive load, compared to near unity displacement power factor and capacitive nature of SMPS with no PFC. However, it has also been shown that the displacement power factor of SMPS with no PFC will be significantly reduced if there are distortions in the supply system voltage, while supply system distortion will have little effect on the displacement power factor of SMPS with passive PFC. Furthermore, it has been show that the harmonic content of the SMPS with passive PFC will be considerably lower than that of the SMPS with no PFC. The SMPS with active PFC will essentially have no harmonic content and will draw no fundamental reactive power from the supply system. All three SMPS sub-type loads will draw constant power, independent of changes in supply system voltage.

An analytical SMPS model has been developed and verified for sinusoidal and non-sinusoidal supply conditions. It has been shown from comparisons with measurements that this analytical model can very accurately predict both harmonic and power demand characteristics of actual SMPS load. Review of key dc link parameter values has led to the development of generic per-unit analytical models of SMPS with passive PFC and SMPS with no PFC. These generic models are able to accurately represent the characteristics of a same sub-type aggregate load, which has been shown via comparisons with measurements. Thus, proposed generic models can be used directly in mixed load type/sub-type aggregate models for further analysis in Chapter 6. Polynomial and exponential models of the three SMPS load sub-types have also been developed and presented in this chapter.

Chapter 5
Lighting loads

5.1 Introduction

A recent survey by the International Energy Agency ([93]) estimated that about 19% of global electricity consumption in 2005 was used for lighting. The contributions of four main load sectors to this figure are: outdoor (stationary) lighting 8%, commercial 43% (or 30% of the total demand in commercial sector), residential 31% (or 18% of the total demand in residential sector), and industrial 18% (or 9% of the total demand in industrial sector). Figures for the UK estimate that the proportion of total energy consumption by lighting loads range from 9%-20% of the total demand, with about 20% and 40% contributions of lighting to the total demand in residential and commercial load sectors, respectively [70]. This chapter focuses primarily on the domestic (i.e. residential) load sector, where four major types of light sources currently in use are: general incandescent lamps (GILs), compact fluorescent lamps (CFLs), and to a lesser extent linear fluorescent lamps (LFLs) and halogen incandescent lamps (HILs). The same four types of light sources are also used in the commercial load sector, where LFLs are more common.

In order to reduce UK's consumption of electrical energy required for lighting, there have been numerous incentives for a wholesale substitution of GILs and other low-efficiency light sources with more efficient LFLs and, particularly in the domestic sector, CFLs. For example, British Gas announced in 2008 that all its customers will receive four free CFLs, totalling around 52 million CFLs. Furthermore, there is a proposal for a voluntary phasing out low-efficiency light sources in the UK between now and 2011, while Ireland has already banned their sale. Similar efforts exist in several other countries, which either passed or are considering the legislation to restrict or ban the sale of GILs (e.g. Australia, Canada, Cuba, New Zealand and Switzerland), while most recently European Commission recommended phasing out GILs between 2009 and 2012). This clearly suggests that the CFLs will become a dominant type of lighting load in the domestic sector in the near future. Therefore, it is important to have simple and accurate load models of these devices for use in power system studies.

This chapter investigates the general characteristics of CFL and LFL loads. It is found that, in a similar way to SASD and electronic dc power supply loads, harmonic legislation will have a large effect on the characteristics of CFLs and LFLs. The effect of this legislation

on modern LFLs results in these loads requiring active PFC, and thus allowing them to be simply represented as constant active power loads in power system analysis. However, the harmonic limits applied to CFLs are less stringent, and a full PSpice circuit model is developed to represent the characteristics of these loads. This full model is verified with measured data, and then reduced to equivalent circuit model. A generic analytical CFL model is then proposed using the information gathered from a review of typical CFL circuit topologies and values of key circuit components. The proposed generic analytical model is able to accurately represent all harmonic and power demand characteristics of a measured aggregate CFL load. Finally, polynomial and exponential interpretations of the proposed generic analytical CFL and simple LFL models are presented and compared to existing load models found in literature.

5.1.1 Previous work on the representation of CFLs and LFLs for power system studies

Although there has been a considerable amount of work on the modelling of both LFLs and CFLs (and associated electronic ballast circuits), the primary focus was on design and efficiency of these light sources. From a "load modelling for power system analysis" point of view, however, there has been a little previous work. In the mid 1990s, the IEEE Task Force for load representation ([3] and [4]) recommended representing these loads as the constant MVA loads. References [15], [94] and [22], on the other hand, proposed an exponential load model for CFL active/reactive power demand characteristics, with parameters (i.e. coefficients and, where presented, displacement power factors) shown in Table 5.1.

Table 5.1: *Previous load model coefficients for CFLs and LFLs.*

Model/Source/year	Light source type	PF_1	Exp. model	
			n_p	n_q
Model 1 [3] 1992	no distinction made	not stated	0	0
Model 2 [15] 1980	FL	0.9	0.96	7.4
Model 3 [22] 1997	CFL	0.97	1.03	0.46
	FL	0.98	0.89	1.21
Model 4 [94] 1994	CFL	not stated	1	0.35
	FL	not stated	1	3

5.2 Fluorescent tubes

5.2.1 General principles of operation

A fluorescent tube is made of two electrodes sealed in a glass tube containing a mixture of mercury and small quantity of an inert gas (typically krypton or argon) at a low pressure. The tube electrodes are coated with a substance, typically Barium or Strontium, that has a low

thermionic emission temperature and therefore will readily emit electrons on warming, i.e. when a current is applied to the electrodes. These emitted electrons act to ionise both the inert gas and mercury atoms in the glass tube, forming a plasma. After initial ionisation, a process of avalanche ionisation will occur, resulting in the rapid increase of the plasma conductivity and (if uncontrolled) increase in current flow through the tube. On ionisation, the mercury atoms emit a photon in the ultra violet region. This ultraviolet light is then converted to the visible spectrum by way of a fluorescent powder, coated to the inner surface of the tube. This physical process results in the tube having a negative resistance characteristics, because as current flow through the tube increases, so does ionisation in the plasma, thus tube resistance reduces due to the increased number of charge carriers.

In order to start the discharge process (i.e. ionisation of mercury atoms) and create conducting arc in the tube, high initial/starting voltage is required. This voltage is called "tube striking voltage", V_{strike}, and is a function of the gas mixture and pressure in the tube, the tube size and the particular type of electrodes used. Typically, V_{strike} will be in the range of 500V to 1200V, [95]. Once the tube is started, the voltage across the tube (referred to as the "tube arc voltage") will decrease and remain at a fairly constant value, normally between 40V to 110V. If the tube electrodes are also heated during the initial ionisation process, the value of V_{strike} can be reduced, what is called the tube pre-heating stage.

Due to the requirement of high tube starting voltage and the fact that tube conductance will increase with current flow (negative incremental impedance), both the tube current and the voltage must be controlled to ensure that the tube operates within specification. Hence, a ballast circuit is used to implement such control between the AC input supply and the tube.

5.2.2 Types of fluorescent tubes

Fluorescent tubes come in a wide variety of shapes and sizes. However, they all operate on similar principles as previously described. The work in this thesis is primarily concerned with modelling those types of fluorescent tubes that are likely to replace traditional GILs. The most common types of GILs used in domestic applications are of rated power 40W, 60W and 100W, respectively making up 20%, 50% and 20% of currently estimated domestic lighting load, [96]. These GILs are expected to be replaced by 8W, 11W and 18W CFLs, as they give similar output lumens. Thus, the majority of this work will focus on CFL with rated power less than 25W.

5.3 Magnetic ballast for LFLs

In order to control the current and voltage of the fluorescent tube, traditionally simple ballast circuits have been used, referred to as magnetic ballast. These ballasts typically consist of a

large value inductor, a capacitor and 'starter switch', Figure 5.1.

On connection of the ballast to the supply system, the tube is off and presents a high impedance path to the current in the ballast circuit. The starter switch consist of a small discharge lamp in series with a bi-metallic switch. The lamp is small, and it can be ignited easily from the system voltage. Once ignited, the small discharge lamp will heat bi-metallic strip and eventually switch-off the starter switch. On switch-off the current flow through the ballast circuit is suddenly interrupted, and a large voltage will be induced across the terminals of the fluorescent tube, igniting the tube. Once ignited, the ballast inductor will act to limit the current flow, and the tube will operate in steady state conditions. The tube will switch off and then re-ignite at every zero voltage crossing of the system voltage, but without further need of the starter switch. This leads to the tube flickering at twice the frequency of the system voltage.

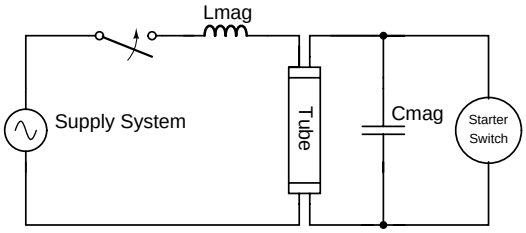


Figure 5.1: *General magnetic ballast circuit.*

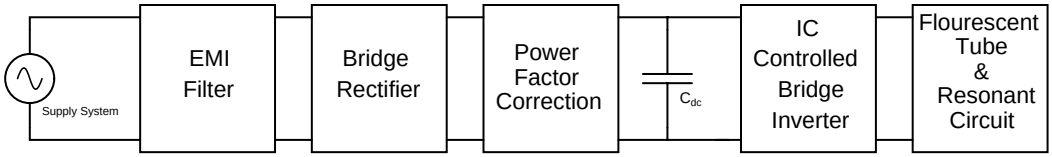
Magnetic ballasts are now generally considered to be obsolete, due to the considerable advantages offered by electronic ballast, which include higher efficiency and more precise control of tube voltage and current, helping to considerably increase tube lifetime. Additionally, the small size of electronic ballast enables "compactness" of CFLs and helps in eliminating flicker. When considering LFL, the ballast is often external to the tube, so it is possible to simply replace the old magnetic ballast with the newer electronic ballast, thus further reducing the number of magnetic ballast present in the system load mix. For these reasons magnetic ballasts are not considered further in this thesis.

5.4 Electronic ballasts for CFLs and LFLs

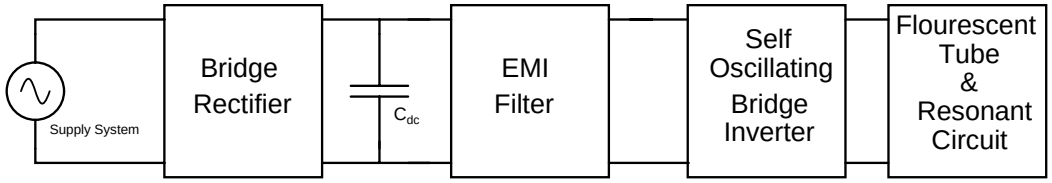
Figure 5.2, shows a general circuit block diagram for the CFL and the LFL. Each of the component blocks shown in Figure 5.2 is now discussed.

5.4.1 Electromagnetic interference

Electromagnetic Interference (EMI) is a term used to describe unwanted high frequency electrical noise, usually generated by rapidly changing currents, e.g., due to the switching



(a) General linear fluorescent lamp ballast.



(b) General compact fluorescent lamp ballast.

Figure 5.2: *General block diagrams of electronic ballasts and tube for LFL and CFLs.*

mode of operation of some electronic circuits [3]. As electronic ballasts are designed to operate in exactly that mode, corresponding switching currents may cause EMI-related problems, and EMI suppression filters must be used. The most common topology of EMI filter filter used in CFLs is shown in Figure 5.3. This topology of EMI filter allows EMI suppression to be achieved with small physically sized components. The EMI circuit often found in LFLs is commonly of the form already discussed in Chapter 4 and shown in Figure 4.3.

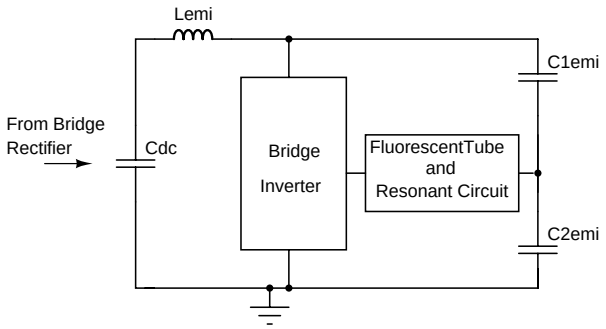


Figure 5.3: *Typical EMI filter commonly found in CFLs.*

5.4.2 Bridge rectifier

The ballast circuit will incorporate a single-phase bridge rectifier, used to convert the input single-phase ac system voltage to dc voltage. The configuration of the bridge rectifier used in an electronic ballast is exactly the same as that of the SASDs (see Section 3.3.1), and thus the principles of operation of this circuit will not be re-discussed here.

The size of the dc link capacitor, C_{dc}, is again related to the power rating of the ballast and after the extensive review of available literature and several manufacturers' specifications/design data, as well as after opening several CFLs, it is found that for the CFL and LFL ballasts with

rated powers from 5W to 40W the common values for C_{dc} are between $1.8\mu F$ and $20\mu F$. Further investigation confirmed that the size of the dc link capacitor is usually selected by the manufacturer, as a trade-off in fulfilling the requirements for harmonic emission, tube lifetime and overall device performance. The size of the capacitor considerably affects the harmonic emissions of the CFL/LFL, and will provide a practical limit for size of C_{dc} with tube rated power. This is discussed in more detail in Section 5.10.

The CFLs will (tend) not use NTC thermistors in their rectifier circuit to provide inrush current protection, unlike previously considered SASD and electronic loads. The reason for this is cost, as the NTC thermistor would represent a considerable expenditure compared to the rest of the ballast circuit. In order to protect the CFL's bridge rectifier from high inrush current, a simple fixed value resistor, R_{in}, is commonly used. Again, from review of available literature and after opening CFLs, it was found that the values of R_{in} varies in the range of about 8-18Ω, with CFLs of higher rated power having larger input resistors. This permanent resistance in the bridge rectifier conduction path will lead to extra losses, which are deemed as an acceptable trade-off compared to cost of including NTC thermistor. This fixed resistance will also have a secondary effect in reducing the rate at which C_{dc} is charged, helping to decrease the harmonic content of the CFL input current.

5.4.3 Bridge inverter

According to [95], 100% of the CFLs/LFLs in Europe use the bridge inverter topology, which is a simple chopper circuit producing a square wave output at a frequency dictated by the driving pulses. There are two major forms of bridge inverter drive circuit: IC-controlled, and self-oscillating. The IC-controlled circuits use pre-fabricated chips to produce required gate pulses, and provide some additional functionality over the self-oscillating alternatives. This increased functionality often includes the ability to dim the tube, detect failure of the tube to strike, detect a damaged tube and control the bridge-inverter in such a way to maximise tube lifetime by careful control of the tube striking voltage and current. The self-oscillating bridge inverter, on the other hand, is a simple circuit, providing no additional functionality beyond supplying the bridge inverter with gate pulses suitable for tube striking, and then normal tube operation. Self-oscillating bridge inverters are considerably cheaper than IC-controlled ones, and as cost is of crucial importance in the highly competitive CFL market, the self-oscillating bridge inverter topology is almost universally used in these applications. The IC-controlled chip, however, is commonly used in LFL applications, where the additional features are often required, making the self-oscillating bridge inverter unsuitable there. Only the self-oscillating ballast circuit is discussed in detail in this thesis, as for the purposes of modelling of CFLs/LFLs ballasts the IC control chip may be simply represented as a fixed frequency square wave voltage source.

5.4.3.1 Self-oscillating ballast

As mentioned, the self-oscillating circuit provides a cheap solution for the production of square wave pulses at high frequency. The main oscillator circuit usually consists of only two bipolar transistors and a toroid with one primary and two secondary windings. Figure 5.4 shows the circuit diagram of a typical self-oscillating circuit, commonly found in CFL. During the oscillation process, the collector current of TR_2 will linearly rise, as will the current flowing through the primary toroid winding, until the toroid core saturates. At that point, the relative permeability of the toroid will become effectively unity, and the base voltage of transistor TR_2 will decrease, eventually switching off TR_2. At the same time, TR_2 base voltage decreases, TR_1 base voltage will increase and therefore TR_1 will be turned on when TR_2 is turned off. This process then repeats for each half-cycle. The oscillation circuit cannot start oscillations on its own, and a starting circuit, made up of resistors R_1 and R_2, diode D_1, Capacitor C_1 and DIAC is required. On initial connection to supply, C_1 is charged through R_1, causing the the voltage across C_1 to rise exponentially. When the voltage across C_1 reaches the breakdown voltage of the DIAC, the DIAC will allow current to flow and hence the TR_2 base will be triggered, starting the oscillator process. As TR_2 turns on each half-cycle, diode D_1 is included to provide a path to discharge C_1, preventing further triggering pulses. The oscillating frequency of this circuit, f_{op}, is dictated by the value of $R_{b1,2}$, the magnetic properties of the toroid core and its turns ratios of the primary and secondary windings.

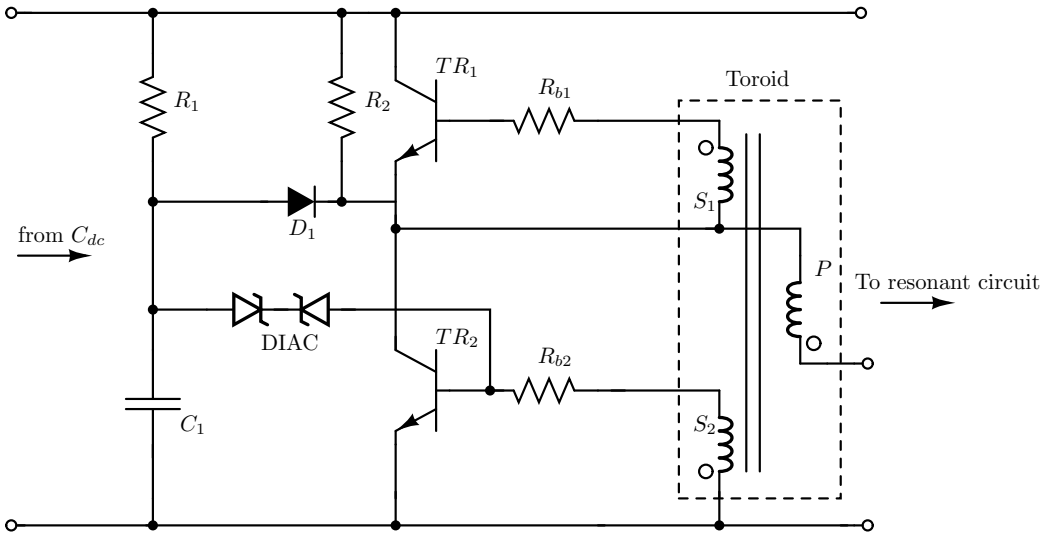


Figure 5.4: *Typical CFL self-oscillating circuit.*

5.4.4 Resonant circuit

The standard method of starting fluorescent tubes is to use the resonant circuit shown in Figure 5.5. The tube is represented by a resistance, which forms an RLC resonant circuit with L_{res} and

C_{res}. On start-up, the tube does not conduct, as its resistance is very high, and lightly damped resonant circuit is formed by a series connection of L_{res} and C_{res}. The resonant operating conditions will cause the voltage across C_{res} to increase rapidly ("pre-heating" of the tube), until the tube striking voltage is achieved and the tube starts to conduct. Once in steady state, the tube effectively turns the resonant circuit into a series LR circuit, and voltage drop on L_{res} will determine the active power taken by the tube.

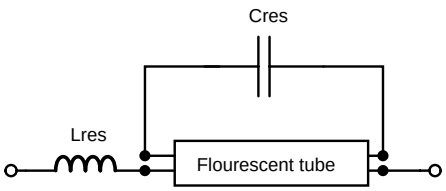


Figure 5.5: *Resonant circuit and fluorescent tube.*

5.5 Representation of fluorescent tube

Previous work on analytical representation of fluorescent tubes was mainly related to the ballast design process (e.g. [97–101]). The corresponding developed steady state tube models were based on the physical characteristics of the fluorescent tube, which are common for both linear fluorescent tubes (LFT) and compact fluorescent tubes (CFT). The main electrical feature of fluorescent tubes are their negative resistance characteristics, which change as a function of power flow through the tube (with resistance decreasing with increase of power). Figure 5.6 shows the typical 'v-i' characteristics of a fluorescent tube operated at different active powers, [97]. It can be seen that the tube 'v-i' characteristics change depending on the power flowing through the tube, where gradient of the 'v-i' characteristic reduces for increased power. Hence, the tube is said to have a negative resistance characteristic, (see also Section 5.2.1). Physical characteristics of LFT can be represented analytically in a number of different ways. This section gives a brief summary of the most common tube models found in the literature.

5.5.1 Previous tube models

Paper [97] developed a cubic expression representing tube instantaneous voltage as a function of tube instantaneous current, (5.1). The coefficients for this cubic expression are of the form shown in (5.2) and (5.3), which in turn are dependent on the average tube power, i.e. the rms tube power, P_t.

$$v_t = A \cdot i_t + B \cdot i_t^3 \tag{5.1}$$

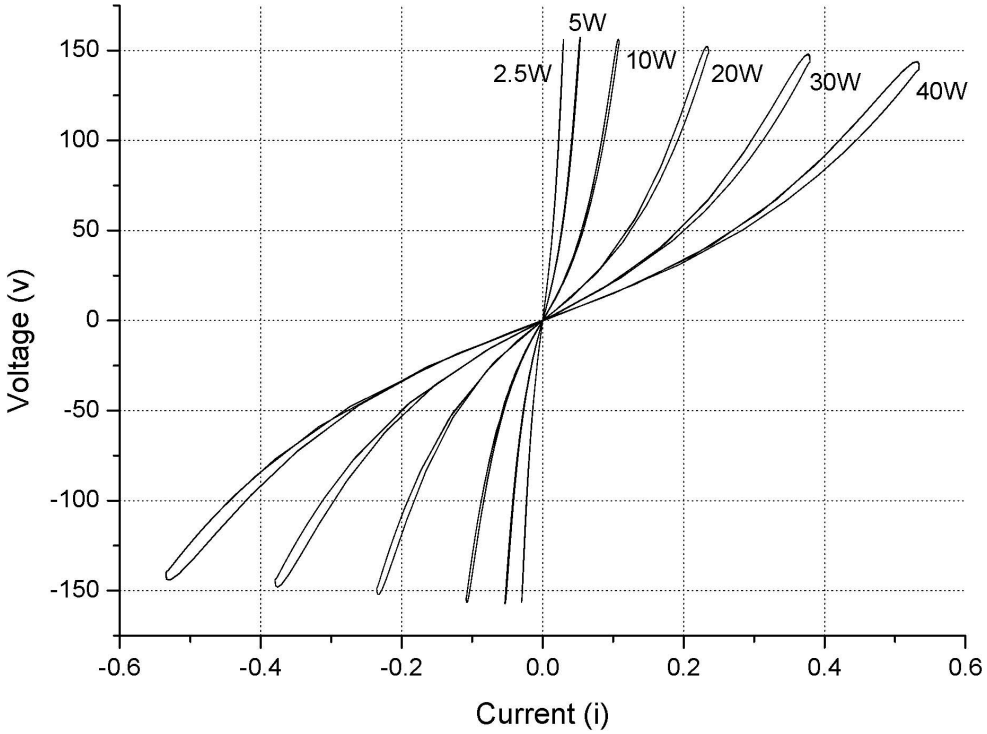


Figure 5.6: *Typical linear fluorescent tube (40 W) 'v-i' characteristics when operated at different active powers, [97].*

where: v_t and i_t are instantaneous tube voltage and current and coefficients A, B are:

$$A = a_1 \cdot (P_t + c_a)^{a2} \tag{5.2}$$

$$B = b_1 \cdot (P_t + c_b)^{b2} \tag{5.3}$$

where: a_1, a_2, b_1, b_2, c_a and c_b are determined experimentally.

Reference [100] uses exactly the same principles as [97], but develops new expressions for (5.2) and (5.3), to enable better fitting of measured data:

$$A = a_1 \cdot (P_t^{-1} + a_2 + a_3 \cdot P_t + a_4 \cdot P_t^2) \tag{5.4}$$

$$B = b_1 \cdot (P_t^{-1} + b_2 + b_3 \cdot P_t + b_4 \cdot P_t^2) \tag{5.5}$$

In [101], the same principles are used, but this time a double exponential model in place of (5.1) is used to represent tube equivalent resistance, R_t:

$$R_t = A \cdot e^{B \cdot P_t} + C \cdot e^{D \cdot P_t} \tag{5.6}$$

where: A, B, C and D are tube specific coefficients, obtained from measurements.

References [102] and [103] use a linear expression in place of (5.1) to represent tube resistance R_t:

$$R_t = \frac{A}{P_t} - B \tag{5.7}$$

where: coefficients A and B are obtained from measurements.

The linear expression (5.7) is commonly used in literature, as it provides a good matching between modelled and measured tube characteristics, while simplifying the tube model. Similarly, [104] and [105] develop tube equivalent resistance as a function of tube current, rather than tube power, while [106] represents tube resistance as a linear function of both current and voltage.

Instead of the instantaneous current and voltage waveforms, references [98], [106], [107] and [108] use the tube rms V-I characteristics to produce the tube model. Figure 5.7 shows the measured V-I characteristics of a typical linear tube from [107]. Again, several different analytical expressions based on this approach have been developed in literature in order to produce the tube model.

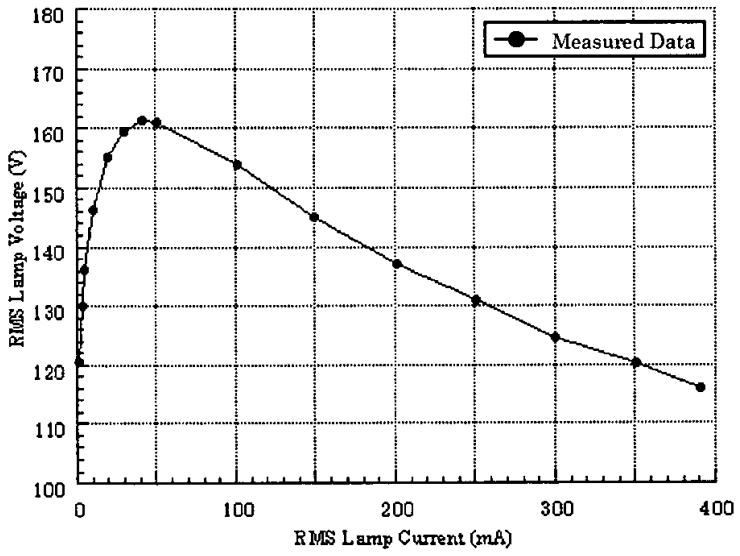


Figure 5.7: *Measured V-I characteristic of a typical linear fluorescent tube (32W), [107].*

In [98], a logarithmic expressions using the tube rms current is applied to derive tube equivalent resistance. This resistance is then used to calculated the tube instantaneous voltage and currents.

$$ln(R_t) = A \cdot ln(I_t) + B \tag{5.8}$$

where: I_t is tube rms current; A and B are coefficients derived from tube measurements.

In [106], the rms current versus voltage characteristic is assumed to be linear, in order to enable the tube model to be developed by measuring only two points of the tube characteristic (at 20% and 100% of rated power). However, the accuracy of this approach is questionable, and not fully justified in the paper.

Finally, [107] presents a tube model with a three-term exponential expression to fit the tube rms current versus voltage characteristic as shown in (5.9). This approach gives the tube rms voltage directly from tube rms current, and can be used to calculate tube resistance, which in turn is used to find instantaneous tube current and voltage.

$$V_t = A + B \cdot e^{(-C \cdot I_t)} - D \cdot e^{(-E \cdot I_t)} \tag{5.9}$$

Where: V_t is tube rms voltage, I_t is tube rms current and $A - E$ are tube specific coefficients.

All of the above described models have generally been formed with LFT in mind, with the exception of [101], which also considered CFT. There has only been limited work that has considered modern CFT, most notably in [108], where an 18W CFT model based on [107] is presented. Apart from the work in [108], it has been extremely hard to find models of modern CFT. Where some work has been done, it has shown that CFT and LFT have very similar characteristics and can be modelled by exactly the same method. Apart from the lack of data for modern CFT, another problem of using previous work (without further verification), is that the tubes have all been characterised by removing them from the ballasts and using a controllable high-frequency square-wave signal generator voltage source to supply the tube. This is obviously not the correct method to characterise CFTs, as they have electronic ballast integrated with the tube. More importantly there will be certain operating regions that the tube would never enter if controlled by a typical ballast, as discussed in the next section.

5.6 Development of new CFL tube model

Because of the lack of CFT models in existing literature, it was decided to measure a number of typical CFTs to determine the general characteristics of fluorescent tubes found in modern CFLs. The power ratings of selected CFLs were chosen as the three most typical found in the UK domestic load category: 8W, 11W and 18W (as discussed in Section 5.2.2).

5.6.1 Experimental set up and method

In order to have precise control over the applied voltage waveform to the CFL ballast, a controllable ac power supply was used , [92]. In order to access the tube terminals, the 'dome' of the CFL was opened, exposing the ballast and tube terminals. Current probes were used to measure the current flowing from the ballast to the tube, i.e. tube current, and also to measure the current flowing from the power supply to the ballast (data used later in this chapter). The tube voltage and ballast input voltage were also measured. An oscilloscope was used to measure and record the voltage and current waveforms (the maximum resolution of the oscilloscope was 2000 data points per output data file).

The measured tube instantaneous voltage and current waveforms can be used to calculate the active power the tube draws from the ballast. As the maximum resolution of the oscilloscope was 2000 data points, it is only possible to capture a few cycles of the tube instantaneous current and voltage waveforms without breaching the Nyquist limit, which would lead to aliasing in the measurements. As the dc link capacitor in CFL ballasts is relatively small, the dc link voltage v_{dc} will contain a relatively large ripple at twice the line frequency, i.e. 100Hz under nominal 50Hz supply conditions. This means that the instantaneous tube voltage and current waveforms will change dependent on the point on the v_{dc} ripple where the measurements are taken, illustrated in Figure 5.8. As the average tube power is required for this analysis, it is necessary to measure the tube instantaneous voltage and current waveforms at four different points, (A - D), on the v_{dc} ripple profile, calculating the associated power at each point and then taking the average power of the four points. Figure 5.8 also shows these measurement points.

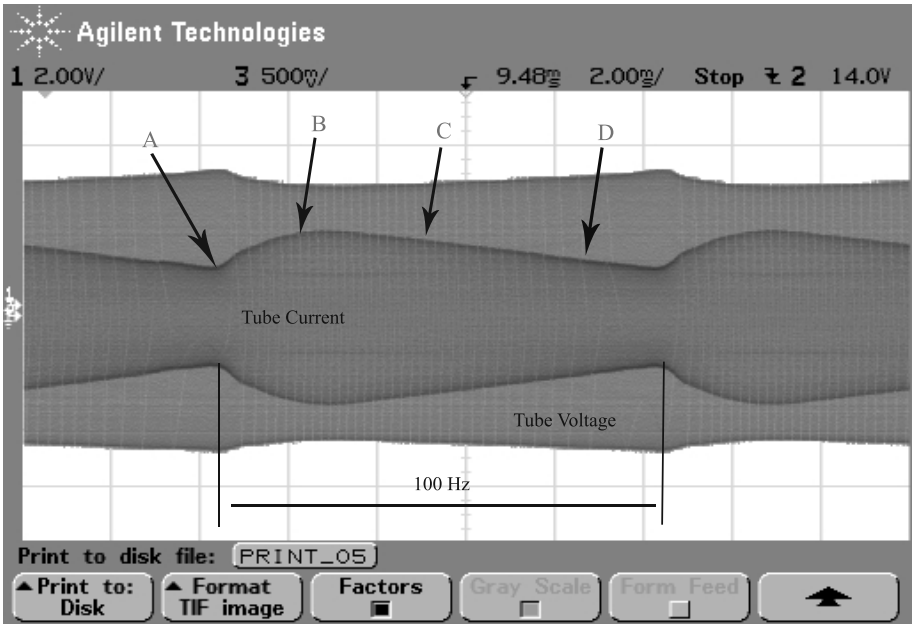


Figure 5.8: *Measured instantaneous voltage and current of CFL 11W tube (electronic ballast output).*

5.6.2 Measured characteristics of modern CFLs

As mentioned, fluorescent tube models in existing literature are obtained by removing the tube from the ballast, and using a signal generator to produce the high-frequency ac voltage and current inputs to the tube. The approach used in this thesis, however, is to control the power delivered to the tube with the connected ballast, as this is the case in real applications.

Another common practice seen in previous work is to characterise the tube between 5% and 120% of nominal operating power. The disadvantage of characterising the tube over such a large range is that the tube starts to exhibit non-linear characteristics when operated at powers below around 30% of nominal power, thus complicating the tube model. However, from the point of view of constructing tube models for use in steady state load supply operating conditions, there is no need to consider the operation of the tube at low powers. This is because the minimum considered input ballast voltage will be 0.8pu, which will result in the tube operating well above 30% of its nominal rated power, normally at around 70% of rated power.

The experimental methods described in Section 5.6.1 were used to measure the instantaneous tube current and voltage waveforms for the three considered 8W, 11W and 18W CFLs. The voltage magnitude applied to the ballasts was altered between 0.8pu and 1.2pu of nominal UK low voltage supply. The rms values of tube current and voltage were calculated from the corresponding measured instantaneous current and voltage waveforms, with tube rms voltage plotted as a function of tube rms current in Figure 5.9.

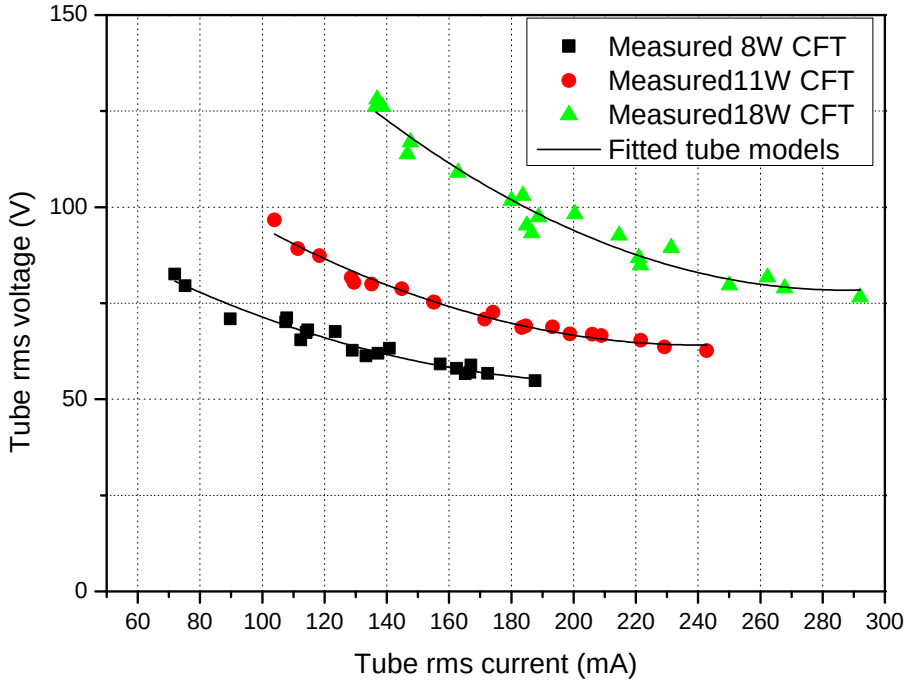


Figure 5.9: *Measured V-I characteristics of modern CFL tubes.*

5.6.2.1 Development of new tube model from experimental results

It can be seen from the results presented in Figure 5.9 that the characteristics of all three considered tubes are very similar. Additionally, these characteristics show similarity to the results obtained in [107] for a linear tube, Figure 5.7. This helps to further support the assumption in [108] that CFT and LFT can be modelled in the same way.

It can be seen from the results in Figure 5.9 that the tube V-I characteristics are not related to each other linearly, but in a quadratic or exponential way. It was decided to use a quadratic form for the new tube model, as exponential functions are more difficult to implement in PSpice software due to issues of convergence. Accordingly, a new tube model of the form shown in (5.10), is proposed. The least square method, described in section 2.7.1, was used to fit the model to the measured data for the three considered tubes. These fits are also shown in Figure 5.9, with the coefficients of the tube model given in Table 5.2.

$$V_t = A \cdot I_t + B \cdot I_t^2 + C \tag{5.10}$$

where: A, B and C are tube specific coefficients.

Table 5.2: *Developed tube model coefficients.*

	Coefficients		
Tube (CFL)	A	B	C
8W	-550	1276	114
11W	-744	1546	154
18W	-1170	2040	247

The proposed tube model determines the tube rms voltage from the tube rms current. This information is then used to calculate the tube equivalent resistance, $R_t = \frac{V_t}{I_t}$. Once the tube equivalent resistance is known, it can be used in conjunction with instantaneous voltage applied to the tube by the ballast to find the tube instantaneous current. The rms value of the tube current may then be used to update the rms tube voltage, and hence the tube equivalent resistance. The process is iterative, with the tube rms current being determined from a running time window integration of the tube instantaneous current. The PSpice implementation of the tube model, (in the form of a schematic diagram), is shown in Figure 5.10.

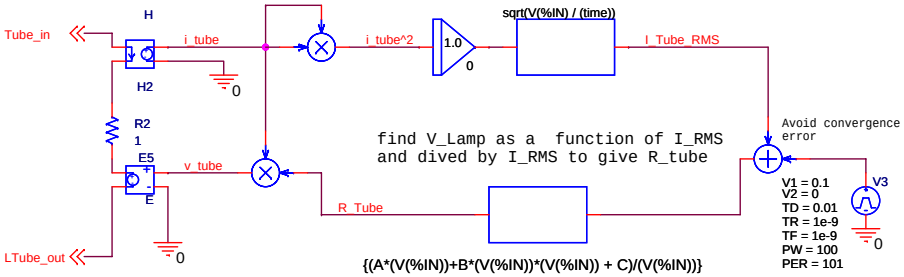


Figure 5.10: *PSpice implementation of the developed tube model.*

5.6.3 Validation of the proposed tube model

As the obtained tube model is developed together with the ballast model, the validation of the tube model is postponed until Section 5.8.1.

5.7 CFL ballast model

The CFL ballast circuit will consist of a EMI-filter, a bridge rectifier, a self-oscillating bridge inverter and a resonant circuit, as discussed in Section 5.4. These circuits, with the exception of the toroid found in the self-oscillating inverter, are made from common components, and can be modelled directly in PSpice software.

The general principles of operation of self-oscillating CFL ballast are also discussed in Section 5.4. In order to properly model the self-oscillating ballast, the magnetic saturation properties of the toroid transformer must be correctly represented, which is a modelling challenge. Additionally, the transistor switches in the bridge inverter must be modelled fully, i.e. not as ideal switches. This is because their actual switch-on characteristics are required to make the model operate correctly.

In order to represent the magnetic saturation properties of the toroid transformer, the saturatable core model developed in [109] was implemented in PSpice. The toroid itself can be considered as a transformer with one primary and two secondaries, for which the turn ratios of both secondary windings are equal. The PSpice model of the developed self-oscillating ballast is shown in Figure 5.11.

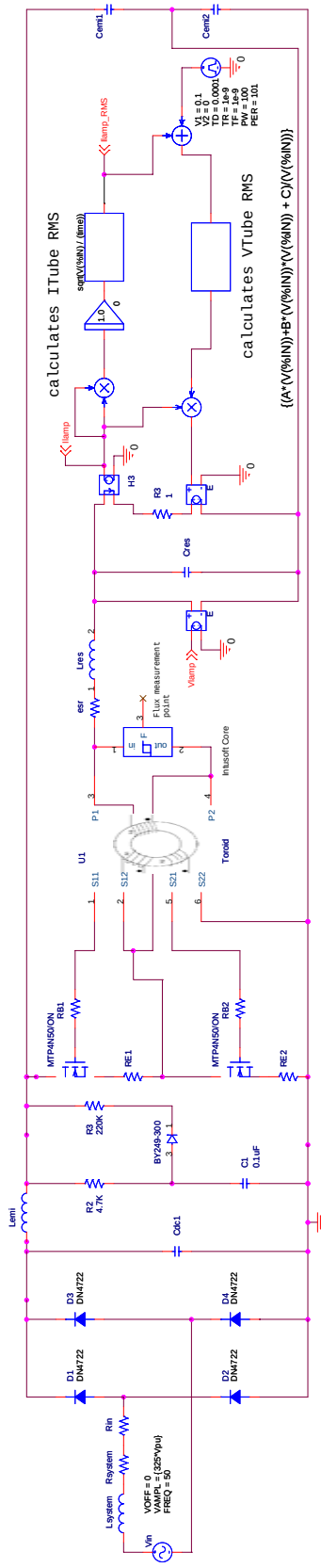


Figure 5.11: *PSpice model of CFL electronic ballast and fluorescent tube.*

5.8 Validation of full circuit CFL model

The self-oscillating ballast and tube models developed in the previous sections were combined and implemented in PSpice, forming a full CFL model. The 11W CFL, previously used to measure tube characteristics (Section 5.6.2) was dismantled, and key components were measured, (i.e. C_{dc}, R_{in}, L_{res} and C_{res}). These measured values are applied directly to the PSpice ballast model. Magnetic hysteresis properties of the toroid in the self-oscillating ballast model were also adjusted in such a way to match the nominal oscillation frequency of the considered 11W CFL ballast which was around 45kHz. In this way, the PSpice full model of the CFL was set up to match a specific CFL.

Although the controllable voltage source, [92], was able to supply a significantly less distorted voltage waveform compared with the normal power lab voltage, its output voltage was found to be slightly distorted. This was attributed to the loading of the CFL. Although this distortion is very low, it still has a noticeable effect on the measured result. It was concluded, therefore, that it is important to faithfully reproduce the actual input voltage supplied to the measured ballast for correct model validation. This is required so any differences between the model and measurements can be attributed to the model, and not due to a differences in supply voltages. To achieve this, the measured output voltage of the controllable voltage source was decomposed into its harmonic elements by means of a fast fourier analysis (FFT) in MatLab. This harmonic spectrum data was then used to accurately reconstruct the output voltage waveform of used voltage source in PSpice, which is then supplied directly to the ballast model.

Simulations were run using the full PSpice 11W CFL model. This model is validated by comparing results of simulations with the results of measurements. As the same modelling approach is applied for all three considered CFLs, (8W, 11W and 18W), the validation is presented only for the 11W CFL, to avoid repetition.

5.8.1 Validation of the developed full PSpice CFL model

The tube instantaneous current and voltage obtained from the PSpice full model were compared to the measured waveforms (11W CFL ballast supplied at 1pu source voltage), Figure 5.12. Further, simulations were performed with the ballast input voltage altered between 0.8pu and 1.2pu. At each point, the rms values of tube current and voltage were calculated, and then compared against the measured data in Figure 5.13. It can clearly be seen from both comparisons that the full PSpice model is able to reproduce the measured results to a high degree of accuracy. These results, therefore, validate the developed CFL tube model and CFL ballast model.

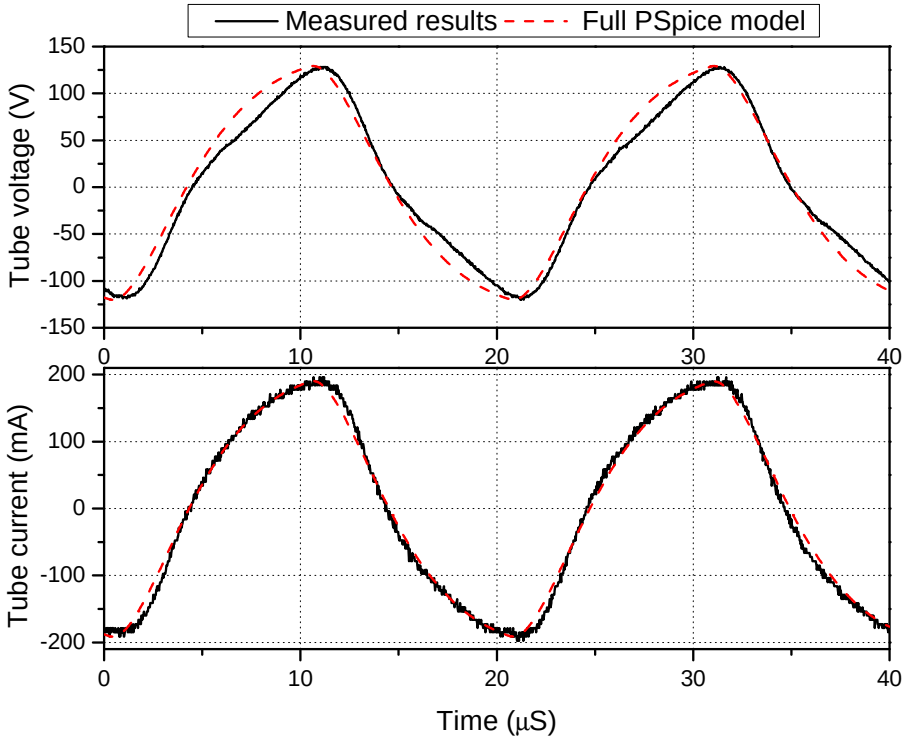


Figure 5.12: *Comparison between measured and simulated instantaneous tube voltage and current waveforms, 11W CFL.*

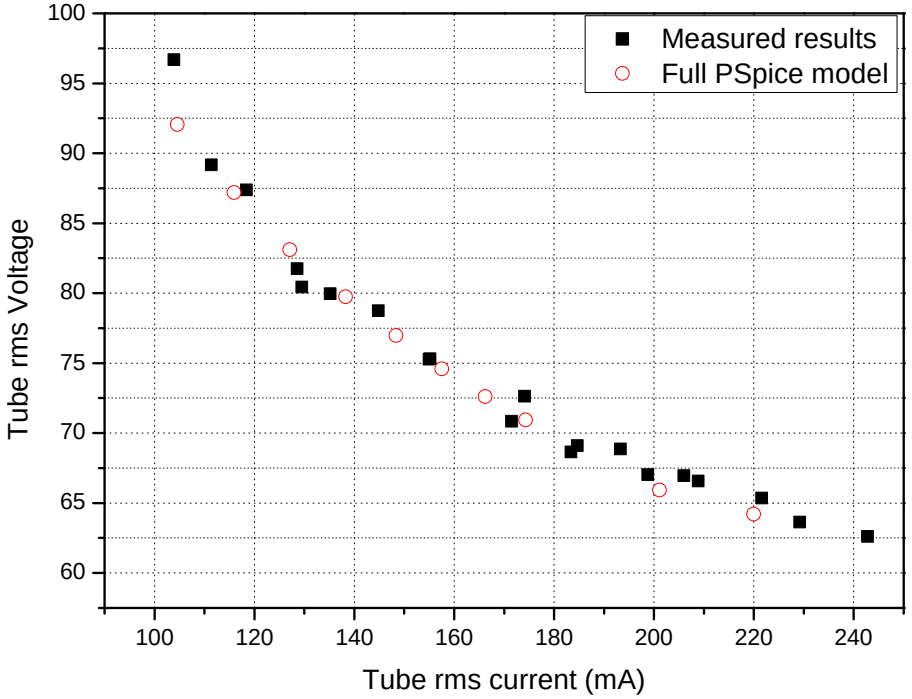


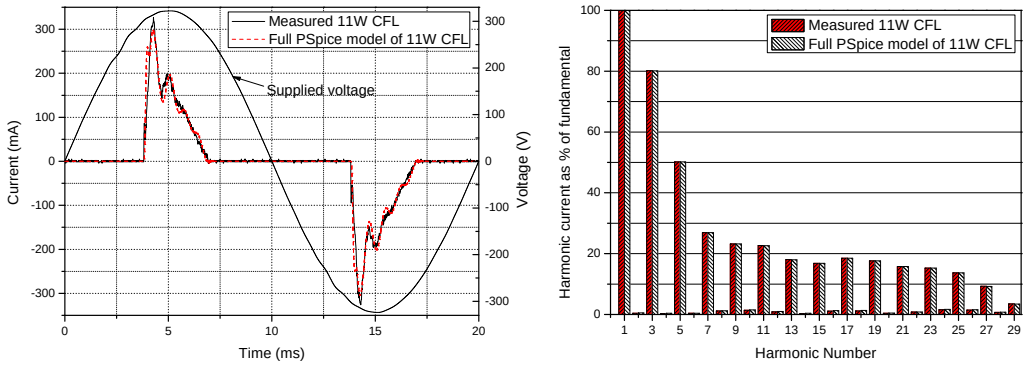
Figure 5.13: *Comparison between measured and simulated rms V-I tube characteristic (11W CFL, for input voltages between 0.8-1.2pu).*

5.8.2 Verification of modelled CFL input characteristics

In order to further validate the full CFL model, its input current and power characteristics are now compared with the measured results. The comparison in Figure 5.14 illustrates the input current waveform and associated harmonic content of the simulated and measured results supplied at 1pu voltage. These results show that the full CFL model is able to accurately predict input current waveform, and hence its harmonic content. Further to these results, Figure 5.15 investigates the ability of the model to predict the P-V and N-V power demand characteristics of the measured CFL. Again, the model performs well with none of the power characteristics showing greater than a 3% error over the input voltage range 0.9 to 1.1pu, and less than 5% error for the full considered range of 0.8pu to 1.2pu.

From the results presented in Figure 5.15, it can be seen that the P-V characteristics of the 11W CFL are linear and follow closely the P-V characteristics of the CFL tube. Therefore, this further justifies the importance of developing accurate CFL fluorescent tube models in the previous section, as the fluorescent tube will dictate the P-V demand characteristics of this load type. It should also be noticed that CFLs are capacitive loads, similarly to lower-power SASDs and SMPS with no PFC. This is because CFLs do not have any additional inductance in their bridge rectifier circuit, as they use other means to comply with harmonic legislation, which is discussed in the next section.

The presented results clearly validate the developed full PSpice model of the 11W CFL. Furthermore, due to the inherent similarity between different CFL types, sizes and powers it is concluded that the developed full PSpice CFL model may be also used as foundation for developing a generic CFL model.



(a) Current/voltage waveforms (b) Current harmonics

Figure 5.14: *Comparison of current waveform and associated harmonic content between measured and simulated 11W CFL.*

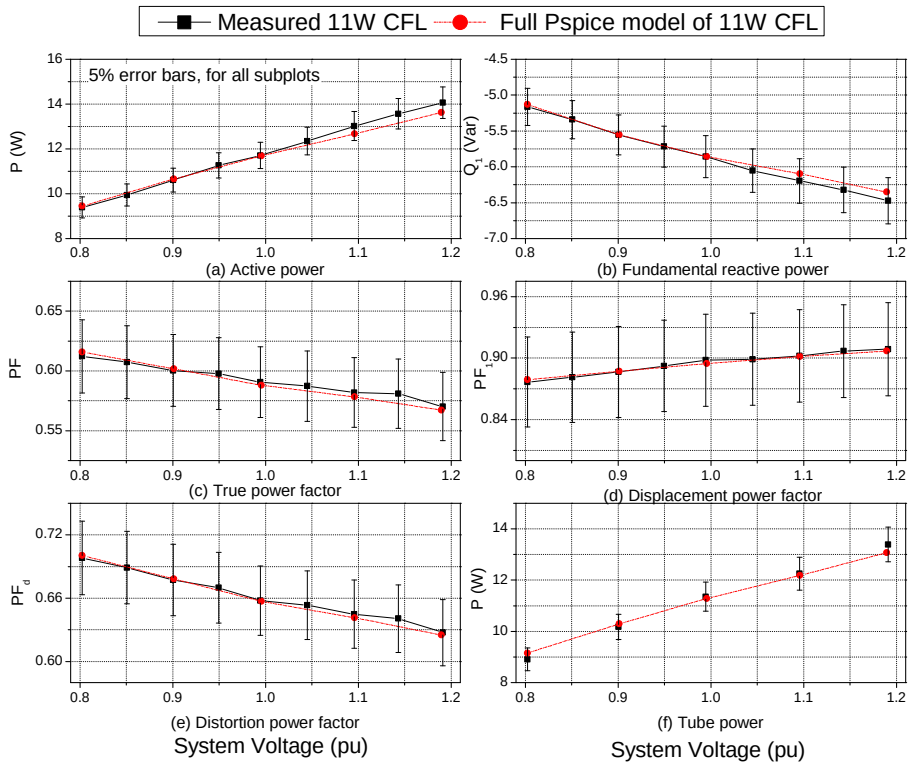


Figure 5.15: *Comparison of active and non-active power demand characteristics between measured and simulated 11W CFL.*

5.9 Effect of system impedance on CFL characteristics

The effect of system impedance on the P-V and N-V power demand characteristics of the 11W CFL considered in the previous section is now investigated. The full PSpice model developed and validated in the previous section was used to produce the P-V and N-V characteristics of the 11W CFL when minimum, nominal and maximum values of system impedance are applied, as defined for a typical distribution system in [42]. Figure 5.16 shows the results of this analysis.

From the results presented in Figure 5.16 it can be seen that the system impedance will have very little effect on the P-V and N-V power demand characteristics of considered CFL. This is because of the presence of the fixed resistance, R_{in}, in the CFL's rectifier circuit (used to provide inrush current protection). The value of this resistor in the considered 11W CFL was measured and found to be 10.2Ω. Therefore, this resistor will dominate the rectifier input impedance, and changes in system impedance will have very little effect on CFL power demand characteristics.

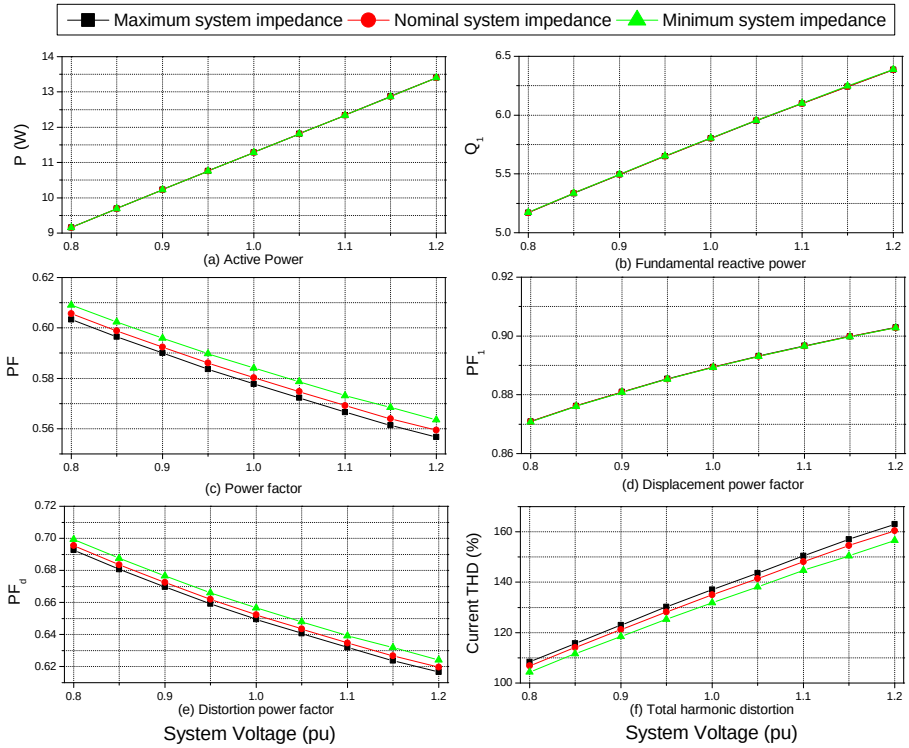


Figure 5.16: *Effect of changing system impedance on CFL active and non-active power demand characteristics.*

5.10 Harmonics

The diode bridge rectifier at the front end of the electronic ballast influences that the CFLs and LFLs draw non-linear current from the supply, rich in harmonics. When considering steady state load models for power system load flow analysis, harmonic emissions might at first glance seem to be of little relevance, but as the discussions in this section will show, legislative harmonic limits play a decisive role in the design, and therefore characteristics, of modern CFL electronic ballasts.

5.10.1 Legislation

The legislative limits that apply to the type of lighting loads considered in this thesis, i.e. lighting loads that draw less than 16A per phase and supplied by a single-phase power supply, are stipulated in [30]. Reference [30] designates lighting loads as class C loads, further divided into lighting loads which draw active power greater than 25W (referred to in the remainder of this work as "higher power lighting loads"), and lighting loads which draw active power less than 25W from the supply system (referred to in the remainder of this work as "lower power lighting load"). Higher power lighting loads must adhere to the harmonic limits shown in column 2 of Table 5.3, (C1). Lower power lighting loads must adhere to either one of the

two sets of harmonic limits laid out in column 3 (C2) and column 4 (C3). The limits for higher power lighting loads are far more stringent than the limits associated with lower power lighting loads. There are various methods that designers of CFLs/LFLs use to meet these harmonic limits. The method implemented depends on the limits to be met, and hence on the rated power of the CFLs/LFLs. Accordingly, CFLs/LFLs in the following text are divided into two general classes: a) CFL/LFLs with rated power below 25W and b) CFL/LFLs with rated power above 25W. As discussed in the introduction if this chapter, CFLs will be by far the most common in the lower-power range, as LFLs with rated powers less than 25W are only rarely used (and where they are used, normally in domestics applications, there is a trend to replace them with CFLs). Therefore, CFLs are assumed as typical representatives of lower power fluorescent lighting loads in the remainder of this chapter.

Table 5.3: *Harmonic current limits for lighting loads, class C [30].*

	Rated Power		
Harmonic number	$> 25W$	≤ 25 W	
n	C1 ($\%^1$)	C2 ($mA\backslash W$)	C3 ($\%^1$)^2
2	2	-	-
3	$30 \cdot pf_1$	3.4	86
5	10	1.9	61
7	7	1	-
9	5	0.5	-
11	3	0.35	-
$13 \leq n < 39$	3	$\frac{3.85}{n}$	-
[1]expressed as a % of fundamental component of input current.			
[2] Further requirement of C3: The input current waveform should begin before or at 60^0, have it last peak (if there are several peaks per half-period) before or at 65^0 and not stop flowing before 90^0, where the zero crossing of the fundamental supply voltage is assumed at 0^0 pf_1 is the displacement power factor.			

5.10.2 Meeting harmonic legislation for CFLs with rated power less than 25W

There are two sets of limits that can be applied to CFLs in this power range, (C2 or C3 Table 5.3), with the CFL manufacturers only obliged to adhere to one of these limits. In order to investigate these limits further, the harmonic contents of the input current waveform, drawn by the full PSpice model of the 11W CFL developed in the previous section, is compared to the harmonic limits C2 and C3. This CFL model is supplied with an ideal sinusoidal waveform at 1pu voltage, and result of the comparison are shown in Figure 5.17.

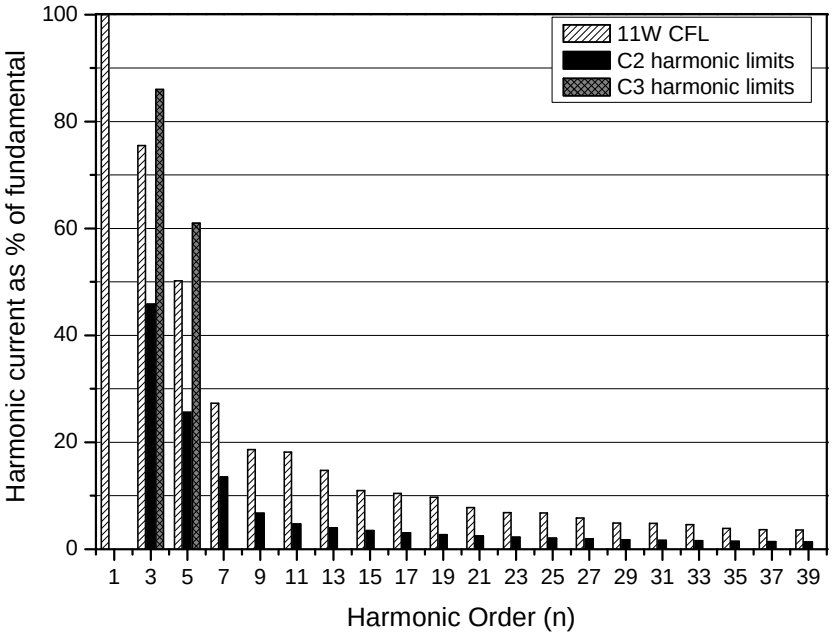


Figure 5.17: *Comparison of harmonic contents of 11W CFL with C2 and C3 harmonic limits from [30].*

The comparison presented in Figure 5.17 illustrates that harmonic limit C3 is far less stringent than limit C2. Therefore, manufacturers will usually aim to meet limit C2 rather than C3. As discussed, the size of the dc link capacitor, C_{dc}, will have a significant effect on the harmonic content of the CFL input current waveform. In order to investigate this influence further, simulations were run using the 11W CFL with different values of C_{dc}. Figures 5.18 and 5.19 show the effect of the value of C_{dc} on the CFL input current waveform and associated harmonics.

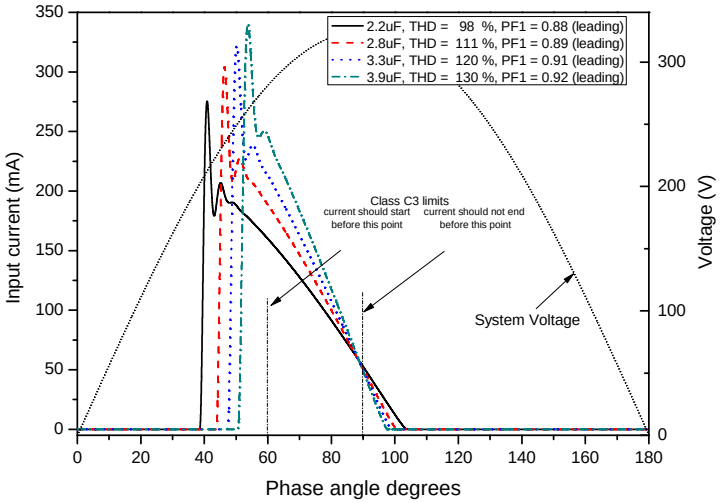


Figure 5.18: *Effect of dc link capacitance on input current waveform of 11W CFL.*

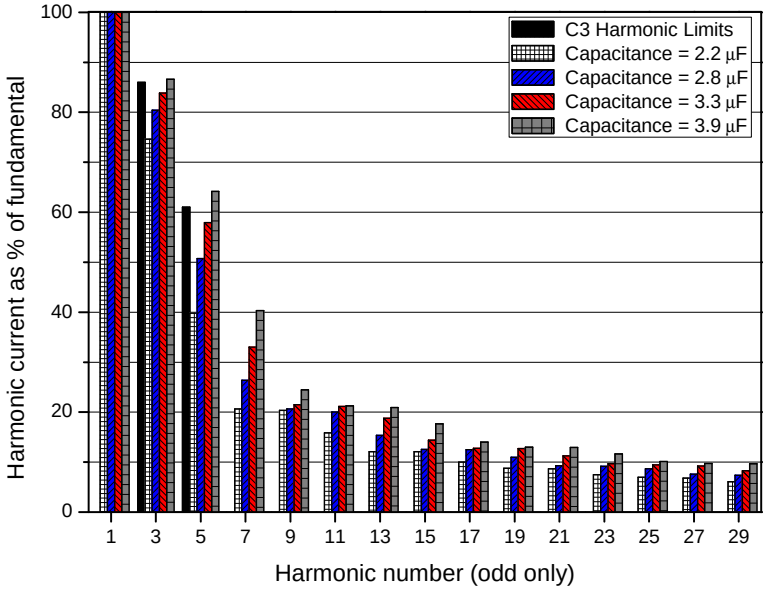


Figure 5.19: *Effect of dc link capacitance on input current harmonics of 11W CFL.*

5.10.2.1 Size of dc link capacitor and harmonic limits

The effect of decreasing dc link capacitance on the input current waveform of the single-phase bridge rectifier has been considered previously in Section 3.3.1. The effects can be again seen in Figure 5.18, which shows that as the value of C_{dc} is decreased, the input current pulses of CFL will shift to the left, have lower peak values and become wider. As the rectifier input current pulse becomes wider its harmonic content will decrease and it will become 'more' sinusoidal. However, as the CFL input current moves to the left, the CFLs' displacement power factor will reduce, and the CFL load will become more capacitive. This is because the current waveform is becoming less symmetrical relative to the system voltage maximum (see also Figure 3.3).

It can be seen from Figure 5.19 that smaller values of dc link capacitor allow for legislative/mandatory requirements (Table 5.3) to be met. Therefore, manufacturers of CFLs tend to use smaller values of capacitors, C_{dc}, to satisfy these harmonic limits. There are also significant cost savings, when smaller capacitors are used to meet harmonic limits, as these are cheaper than the larger ones, and there is no need to include extra circuity for power factor correction in the ballast.

Lower capacitor values, however, will increase dc link voltage ripple and also lead to increased fundamental reactive power flow in the supply system. The increased fundamental reactive power, however, is not a concern of the CFL manufactures, as there are currently no legislative limits in place stipulating minimum values of displacement power factor. However, the increased voltage ripple will also have an effect on the CFL design, as is discussed further.

5.10.2.2 Size of dc link capacitor and dc link voltage ripple

The crest factor of a fluorescent tube current is defined as the ratio of the rms tube current to peak tube current, (5.11). The higher the tube crest factor, the more electrical stress will be imposed on the tube, having a particular influence on tube electrodes and shorting of the tube lifespan. Manufacturers of fluorescent tubes generally specify that tube crest factor should not exceed 1.7 in normal operation([110], [111]), if the tube is to operate within the specified lifetime.

$$CF = \frac{I_{lamp}, peak}{I_{lamp}, RMS} \tag{5.11}$$

In the case of CFTs/FLTs controlled by electronic ballast, the tube crest factor is directly proportional to the dc link ripple voltage, and hence the size of C_{dc}. This is because dc link voltage ripple is directly translated, through the bridge inverter, to the tube.

5.10.2.3 Size of dc link capacitance, and compromise between harmonic limits and crest factor

From the previous discussions, it can be concluded that the size of the dc link capacitor found in the ballast circuit of CFLs will be selected based on a compromise between meeting specified harmonic limits while not excessively compromising the tube lifetime. These two criteria define upper and lower limits for the size of C_{dc} in modern CFL applications.

Simulation models of 8W, 11W, 15W, 18W, 20W and 25W CFLs were developed in PSpice software. The standard self-oscillating ballast was used in all these models, with appropriate typical ballast component values. The tube models of the 8W, 11W and 18W CFLs were developed from measurements, in exactly the same was as presented in Section 5.6.2.1. The tube models of the 15W, 20W and 25W were taken directly from those developed in [98]. The applied voltage to the ballast was an ideal sinusoidal waveform at 1pu voltage magnitude and frequency.

For each of these CFL models, the value of C_{dc} was systematically altered with respect to discussed limits. Firstly, the minimum value of C_{dc} for each CFL was ascertained by reducing the value of C_{dc} until the tube crest factor exceeded 1.7, which was found to correlate to a 50% dc link voltage ripple. Each time C_{dc} was altered, the ballast circuit was also adjusted to keep the tube power constant. Secondly, the maximum value of C_{dc} based on harmonic limits was found, again altering the value of C_{dc}, but this time increasing the value until the harmonic limit C3 is just breached, with power drawn by the tube kept constant as before. These two criteria provide practical upper and lower limits for the value of C_{dc} in CFLs. Figure 5.20 shows upper

and lower limits as a function of CFL rated power. Also shown in Figure 5.20 are the values of actual capacitor values found from opening CFLs.

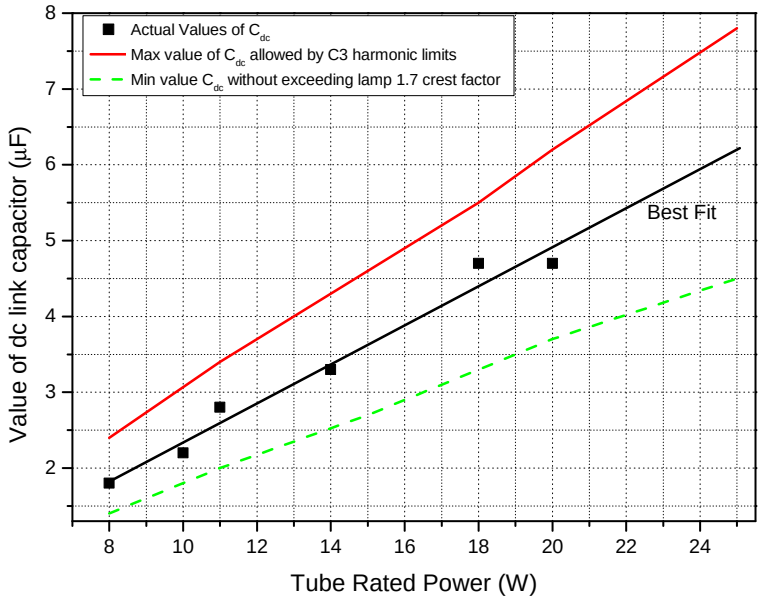


Figure 5.20: *Relationship between the size of dc link capacitor and rated power of CFLs* $\leq$*25W.*

The actual values of C_{dc} found in considered CFLs, shown in Figure 5.20, all lie between the upper and lower C_{dc} limits, which helps to further verify that manufacturers indeed use these limits during the design. A best fit line is also shown Figure 5.20. This line represents the typical expected value of C_{dc}, based on CFL rated power. Next, the typical per-unit reactance value of C_{dc} may be found by selecting a point on this line of best fit, for example 14W and 3.37 μF. This value of capacitance is then converted to a per-unit reactance, by implementing (5.12), which gives $X_{Cdc} \approx 0.25$ pu.

$$X_{Cdc,pu} = \frac{\frac{1}{C_{dc} \cdot \omega}}{\frac{V_{phase}^2}{P_{CFL}}} = \frac{\frac{1}{3.37 \times 10^{-6} \cdot \omega}}{\frac{230^2}{14}} \approx 0.25pu \tag{5.12}$$

where: V_{phase} is the input phase voltage, P_{CFL} is the rated power of the CFL, $\omega = 2\pi f$, where f is the system frequency.

Figure 5.20 represents an important result for this work, as it enables the selection of typical nominal dc link capacitance based on the rated power of the CFL, which as shown before, is a necessary input data for deriving accurate generic per-unit models of these loads.

5.10.3 Meeting harmonic legislation for CFLs and LFLs with rated power greater than 25W

The harmonic limits for CFLs/LFLs with rated active powers above 25W are far more stringent than those applied to lower power CFLs/LFLs. It is not possible to meet C1 limits (Table 5.3) by simply reducing the value of the dc link capacitance. Therefore, additional power factor correction (PFC) circuitry is required to conform to C1 limits. As discussed previously, the PFC circuits can be divided into two general types: passive PFC, and active PFC, which are both discussed below.

5.10.3.1 Passive power factor correction

It is very difficult to meet C1 harmonic limits with passive PFC techniques. Furthermore, passive PFC leads to high tube crest factors. Therefore, passive PFC techniques generally tend to be avoided in modern electronic ballasts. However, where space is an important design requirement, for example in CFLs with rated power above 25W, passive PFC may be found. However, higher power CFL are very uncommon, and therefore passive PFC applied to CFLs/LFLs will not be considered further in this thesis.

5.10.3.2 Active power factor correction

Active PFC has already been described in Section 3.6.1.1. In that discussion, it was noted that the output voltage of the power factor controller is a constant dc voltage, even with relatively large changes in system voltage (0.8-1.2pu). Thus, the voltage to the bridge inverter used stay constant with changes in system voltage and the tube will draw constant active power and will be unaffected by changes in system voltage, as long as these changes are within the operational range of the PFC circuit. Also, as the ballast input current waveform is sinusoidal and in phase with the system voltage, the true power factor of the CFLs/LFLs with active PFC is essentially unity. Accordingly, CFLs/LFLs with active PFC may be very simply represented as linear constant active power loads for the purposes of steady state load modelling.

5.11 General characteristics of CFLs and LFLs

5.11.1 CFLs and LFLs with rated active powers above 25W

As discussed previously in the harmonics section, CFLs and LFLs ballasts powering fluorescent tubes above 25W rated active power are expected to include active PFC circuitry due to harmonic legislation. When an active power factor correction circuit is present, the CFLs/LFLs

will draw constant active power, regardless of changes in input supply voltage and will draw effectively no reactive power.

5.11.2 CFLs and LFLs with rated active powers below 25W

From previous discussions, fluorescent light sources in this power range are assumed to be CFLs. A total of 19 CFLs with different rated powers were measured using the test bed described in Section 5.6.1. The chosen lamp ratings were again 8W, 11W and 18W, as these are the most commonly found CFLs in the residential sector. As far as possible, the lamps were purchased from different locations in Edinburgh area, to try and get a spread of lamps from different manufacturing batches. In the 8W CFL category, six CFL were measured: three manufactured by Philips and three by Osram. In the 11W category, seven CFLs were measured, but this time all the lamps were Philips lamps. Finally, in the 18W category, six CFL were measured, again all were Philips lamps.

The input voltage to the CFLs was altered between 0.8 and 1.2pu, and the ballast input current was measured at each voltage. From the ballast input current and voltage waveforms, the active power characteristics of the CFLs were calculated. The changes in per unit active power characteristics with changes in system voltage for all measured lamps are shown in Figure 5.21, using corresponding CFL, rated active powers as the base power. Also shown in Figure 5.21 is the best fit line obtained (using previously described least square fit method) of the measured results, with $\pm$ 10% error bars.

It can be seen that the P-V characteristics of CFLs of the same rated power and even the same manufacture will vary within around 6-7 % in relation to each other. This results is similar to the findings in [103], which found a similar variance within 10%. From the presented results, it can be seen that the variance between P-V characteristics of CFLs of same rated power is very similar to the variance between CFLs of different rated powers. Therefore, a single per unit generic P-V characteristic may be used to represent the P-V characteristics of CFLs with rated power less than 25W, representing the vast majority of CFLs. This generic characteristic is the best fit line in Figure 5.21.

5.11.2.1 Generic tube model development

In order to developed and implement generic model of CFLs, a generic tube model is required first, as the tube dictates the shape of the CFL P-V characteristic. The tube model developed in Section 5.6.2.1 is used for this generic tube model. The only difference is that rather than representing an actual tube, this model is used to represent the fictitious generic tube. Accordingly, coefficients A, B and C rather than being fit to a measured tube V_{rms}, I_{rms}

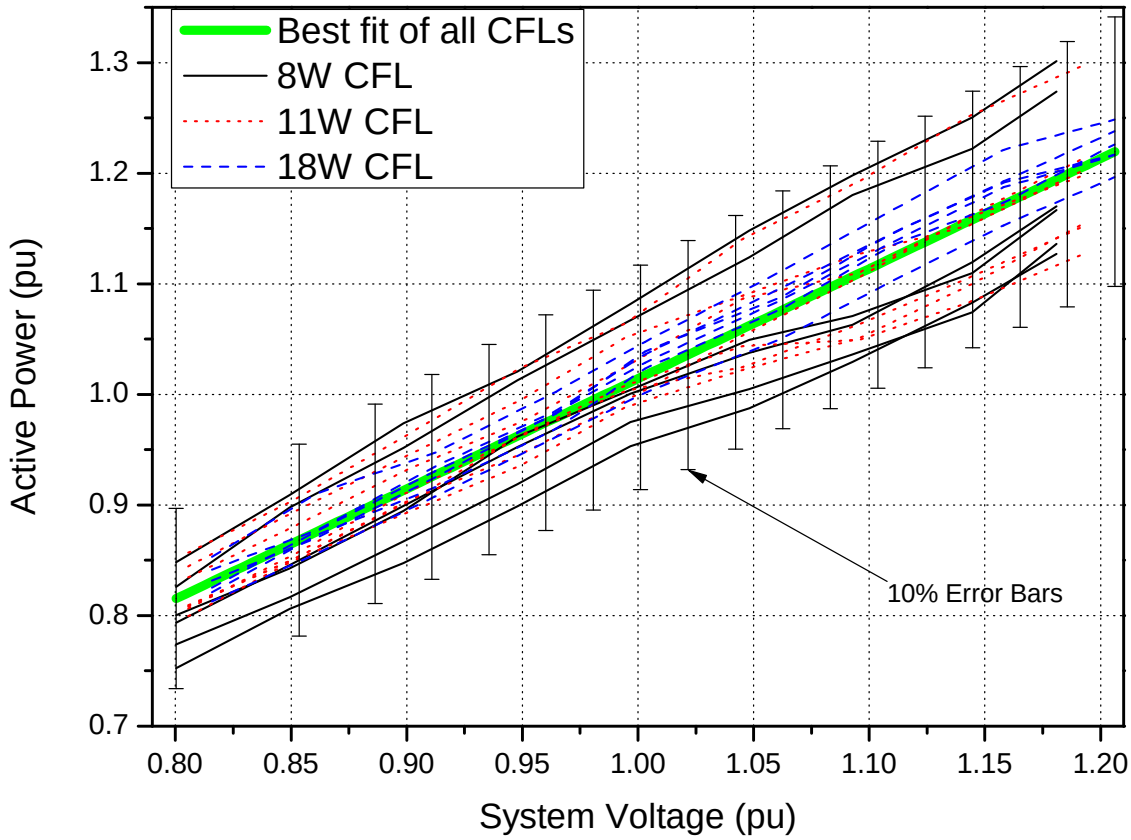


Figure 5.21: *Per unit active power demand characteristics for three most common types (rated powers) of CFLs.*

characteristic, are selected in such a way to provide required generic P-V characteristic, when the tube model is driven by a ballast model. For the development of the generic tube model, the previously considered 11W CFL ballast circuit model is used, as it represents a typical CFL ballast circuit. Simulations were run using the 11W CFL model, with its tube model coefficients A, B and C adjusted until the ballast's P-V characteristics matched the desired generic P-V characteristic. Based on this, full generic CFL model is established. As the basic topology of the self-oscillating ballast is common across all CFLs (due to use of typical components), the 11W CFL ballast and the generic tube model can be directly transformed into a per unit representation, allowing for the representation of aggregate CFLs load and individual CFL instances, what is performed later in this chapter.

5.12 Development of equivalent circuit model for CFL with rated active power less than 25W

So far, full ballast and tube models representing specific CFL have been developed and validated with measured data. As well, a full 11W CFL with generic tube model has been

developed. These developed models are very accurate, but take significant time to simulate due to their complexity. Therefore, they are not appropriate for the further aggregation with same type or other type loads. In the same way as in other chapters of this thesis, this section develops an equivalent circuit model of CFL loads. However, the equivalent circuit model of the CFL is more complicated than that of the other considered non-linear load types, due to the distinctively complex electrical properties of the fluorescent tube.

5.12.1 Development of equivalent circuit CFL model

A circuit schematic of the full and equivalent CFL models is shown in Figure 5.22. To produce the equivalent model, the area marked by the dashed-line box in the full model is reduced to a simple variable resistance. If this area is considered as a 'black box', the relationship between the black box input, which will be the instantaneous dc link voltage, v_{dc}, and the 'black box' output, which will be the instantaneous dc current, i_{dc}, must be found. This relationship will determine the equivalent resistance model. The following investigation is performed using the 11W CFL with generic tube, which is then converted to a per unit representation at a later stage, to form generic CFL model.

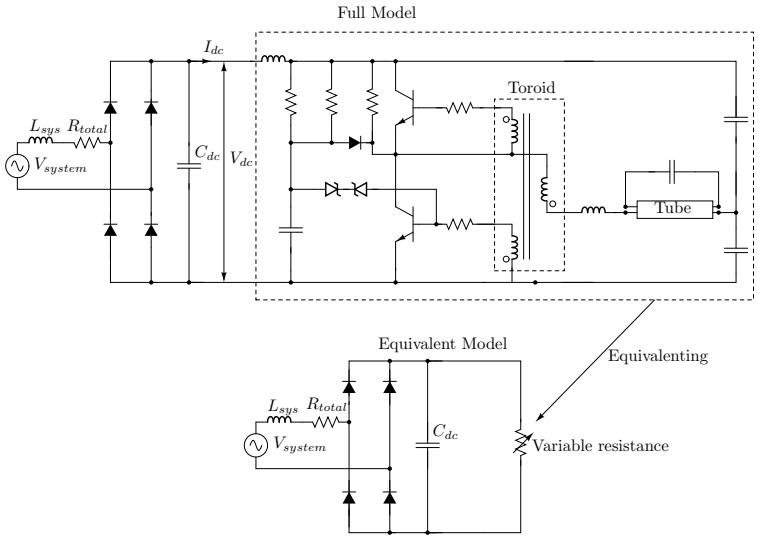
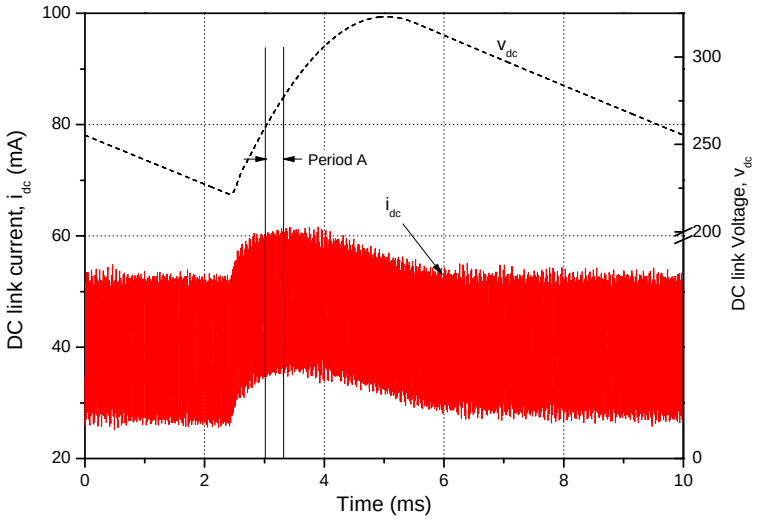


Figure 5.22: *Equivalent circuit CFL model.*

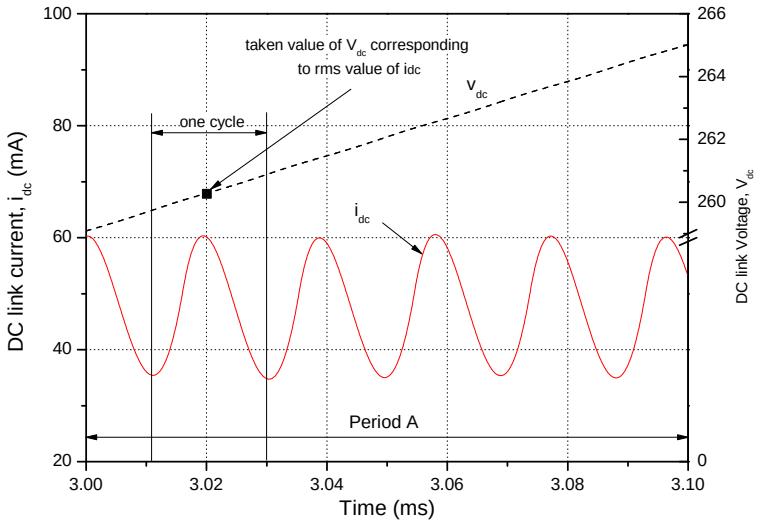
5.12.1.1 Relationship between input voltage and current output at 1pu input voltage

The instantaneous dc link current and voltage waveforms, i_{dc} and v_{dc}, are shown in Figure 5.23, for the ballast supplied with 1pu system voltage. These waveforms are shown over half a cycle of the fundamental frequency in Figure 5.23(a), with Figure 5.23(b) showing a close-up view of i_{dc} and v_{dc} during period A. It can be seen that the envelope of i_{dc} is affected by v_{dc};

i_{dc} increases when v_{dc} is increasing, i.e. when C_{dc} is charging, and then remains seemingly constant when C_{dc} is discharging.



(a) i_{dc} and v_{dc} for one half cycle of fundamental



(b) i_{dc} and v_{dc} individual cycles

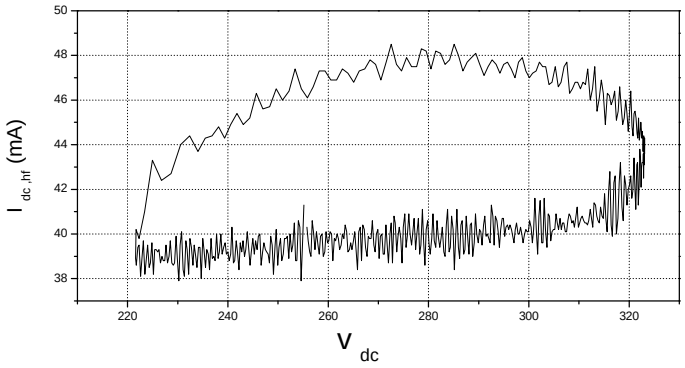
Figure 5.23: *Generic CFL dc link current and voltage waveforms*

A more useful approach to help determine the relationship between i_{dc} and v_{dc} (i.e. to determine equivalent variable resistance) would be to plot them as a function of each other. But for that plot to make any sense, the cycle-by-cycle rms value of i_{dc} should be plotted against the instantaneous value of v_{dc} (as v_{dc} does not oscillate), where the cycle/period time is determined by i_{dc} as shown in Figure 5.23(b). However, i_{dc} will not oscillate at constant frequency, as it is determined by the ballast oscillation frequency, which varies with dc link voltage in the range of around 29-55kHz.

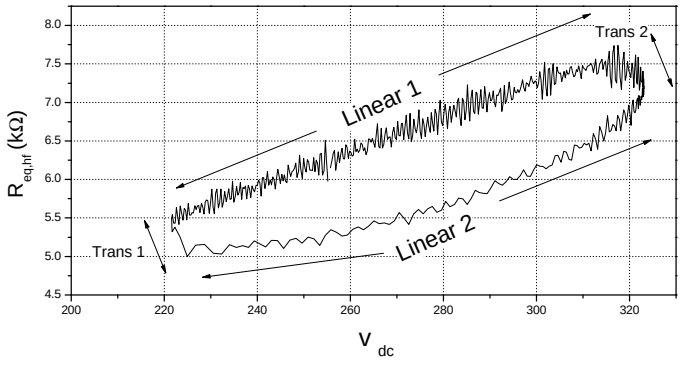
In order to calculate the cycle-by-cycle rms value of i_{dc} a MatLab code was developed that

identifies changes in gradient in i_{dc}. This information is then used to define the cycle time, and hence the period over which to perform the rms calculation of the i_{dc}. This code can be found in Appendix C.1.1. The developed MatLab code was used to process the results presented in Figure 5.23, to produce a plot of $I_{dc,hf}$ (the cycle-by-cycle rms dc link current, i.e. high frequency rms value of dc link current) versus v_{dc} , Figure 5.24(a). As each cycle of i_{dc} is reduced to a single rms value the same must be done for v_{dc} so that the two quantities may be plotted as functions of each other. Accordingly, the value of v_{dc} is taken as the 'middle' value v_{dc} in the considered cycle as shown in Figure 5.23(b).

The parameter of most interest in this analysis is the value of the equivalent resistance that could be used to represent the equivalent loading of the 'black box', i.e. the value of the resistor that would match actual $I_{dc,hf}$ when given v_{dc} is supplied at the dc link. In order to visualise (and aid further analysis) how such an equivalent resistance would vary with v_{dc}, the values of v_{dc} were divided by the corresponding values of $I_{dc,hf}$ using ohms law to give $R_{eq,hf}$. Figure 5.24(b), shows the plot of $R_{eq,hf}$ versus v_{dc}.



(a) DC link current



(b) Equivalent resistance

Figure 5.24: *DC link characteristics of generic CFL model.*

The results presented in Figure 5.24(b) show a relationship/plot between $R_{eq,hf}$ and v_{dc} similar to a hysteresis characteristics. It is immediately clear that the plot is made up of two roughly linear regions, with two transitions between these regions. In order to explain the shape of this

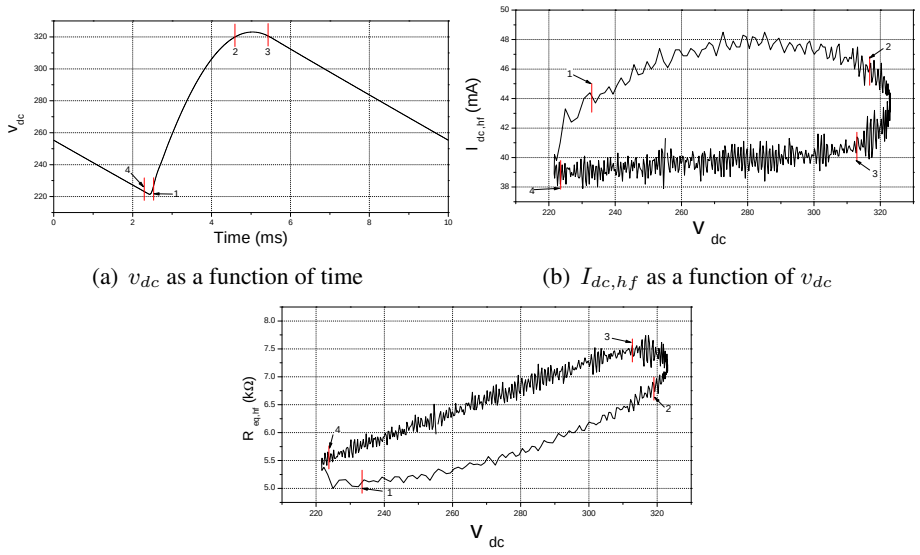
characteristic, it is useful to plot v_{dc} as a function of time, comparing this with the $R_{eq,hf}$ versus v_{dc} characteristic. Such a plot is shown in Figure 5.25, marked clearly with four characteristic points that represent the boundaries between the regions in the $R_{eq,hf}$ versus v_{dc} characteristic. This is further discussed below:

Points 1 - 2 In this region, C_{dc} is charging and dc link voltage is increasing; $I_{dc,hf}$ is fairly constant, varying by only about 5mA. As $I_{dc,hf}$ is fairly constant and v_{dc} is increasing in a nearly linear way, $R_{eq,hf}$ will also increase in the same near linear manner.

Points 2 - 3 This is the transition from the C_{dc} charging to C_{dc} discharging state.

Points 3 - 4 In this region, C_{dc} is discharging and the dc link voltage is decreasing; $I_{dc,hf}$ is essentially constant with changes in v_{dc}. Therefore, $R_{eq,hf}$ will reduce in a linear way with v_{dc}

Points 4 - 1 This is the transition from the C_{dc} discharging to C_{dc} charging state.



(a) v_{dc} as a function of time

(b) $I_{dc,hf}$ as a function of v_{dc}

(c) $R_{eq,hf}$ as a function of v_{dc}

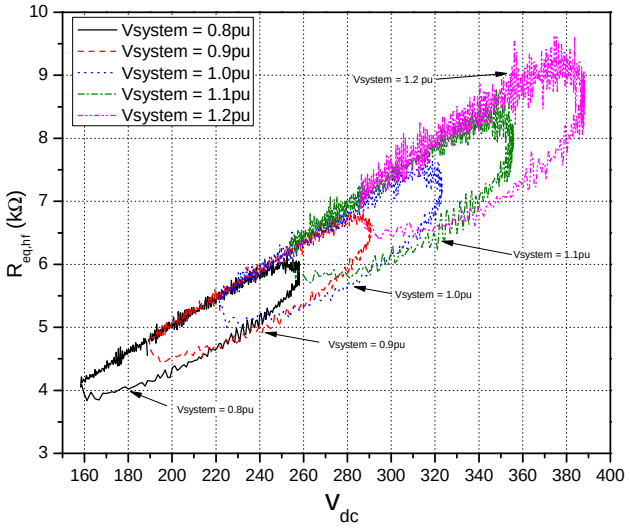
Figure 5.25: *Linearisation of $R_{eq,hf}$ characteristic for generic CFL model.*

5.12.1.2 Extending characterisation beyond 1pu input voltage

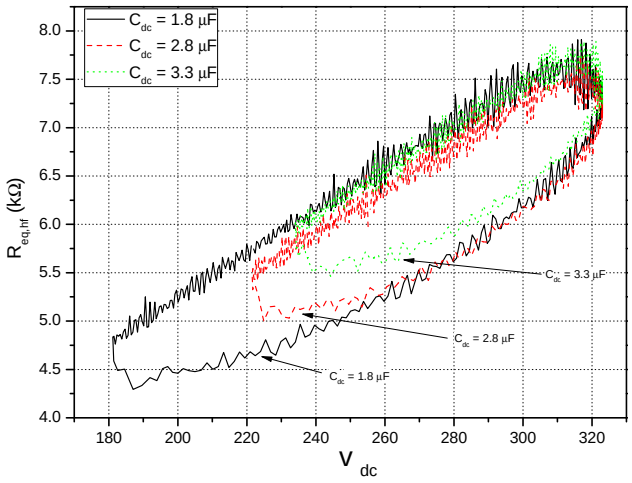
The analysis of the equivalent load so far has only considered the situation where the ballast is supplied with 1pu system voltage. By using exactly the same methodology as discussed above, Figure 5.26(a) is obtained, showing the results of the analysis when the ballast is supplied with 0.8 to 1.2pu system voltage. The results for different input voltages show the same general characteristics as those for the ballast supplied at 1pu, with only a very slight loop widening at higher system voltages, which is due to increased losses in the ballast. Additionally, when ballast pu input voltage is altered, the values of the maximum and minimum dc link voltage

will shift accordingly, but the difference between these values (i.e. the dc link voltage ripple), will remain relatively constant.

Finally, in the analysis so far, the value of C_{dc} has been kept constant at the nominal expected value derived from Figure 5.20, which is $2.8\mu F$ for the generic 11W CFL. In order to produce a more general results, simulations were run with the ballast supplied with 1pu system voltage and values of C_{dc} selected as the maximum and minimum expected values, i.e. $1.8\mu F$ and $3.3\mu F$ respectively. These results are shown in Figure 5.26(b). As expected, the smaller values of C_{dc} lead to a wider variation in v_{dc} over the half-cycle, while larger values of C_{dc} lead to less ripple in v_{dc}. Again, the results also show that change in the value of C_{dc} does not alter significantly the general characteristics of the equivalent resistance.



(a) Change of system voltage (0.8-12.pu)



(b) Change of size of C_{dc} (1pu system voltage)

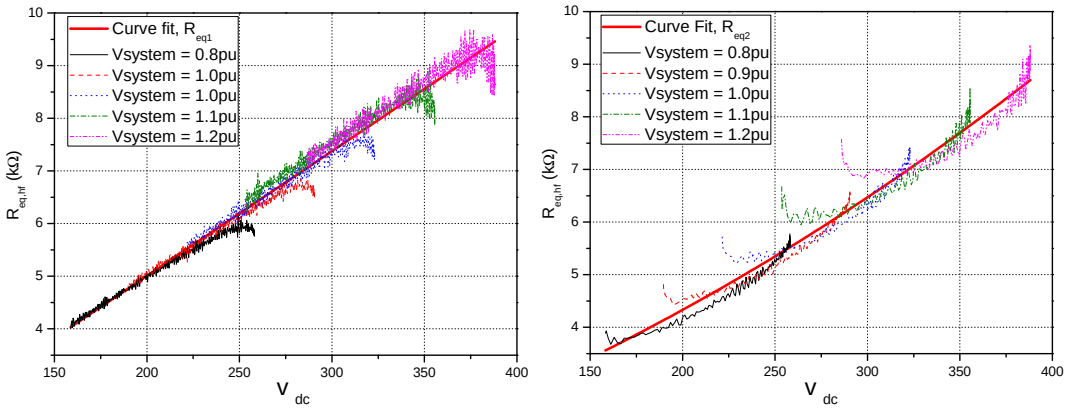
Figure 5.26: *Change of characteristics of equivalent resistance with changes in system voltage and value of C_{dc} in the generic CFL model.*

5.12.1.3 Equivalent resistance as a function of V_{dc}

From the analysis presented so far, it has been shown that the $R_{eq,hf}$ versus v_{dc} characteristic of the generic ballast model consists of two distinctive regions, defined by charge/discharge state of the dc link capacitor. Accordingly, two functional relationships must be developed for expressing $R_{eq,hf}$ as a function of v_{dc} in the equivalent load model. In order to determine these two functional relationships, the results presented in Figure 5.26(a) are split into the two corresponding regions: capacitor charge and capacitor discharge, as shown in Figure 5.27. It can be seen from Figure 5.27 that $R_{eq,hf}$ can be generally expressed as a function of v_{dc} using a second order polynomial expression of the form $y = A \cdot x + b \cdot x^2 + c$ for the charging characteristic, and a linear expression for the discharging characteristic. If the equivalent resistance during the discharge period is defined as R_{eq1} and then during the charge stage as R_{eq2}, expressions given in (5.13) and (5.14) may be developed from fitting the second order polynomial equation to the results of the analysis, as also shown in Figure 5.27.

$$R_{eq1} = 23.7 \cdot v_{dc} + 274 \tag{5.13}$$

$$R_{eq2} = 11 \cdot v_{dc} + 0.021 \cdot v_{dc}^2 + 1300 \tag{5.14}$$



(a) Discharge characteristic (b) Charge characteristic

Figure 5.27: *Equivalent resistance of 11W CFL with generic tube model for two corresponding operating stages.*

5.12.2 Validation of the equivalent resistance model

In order to validate the developed equivalent resistance model, the functional expressions for R_{eq1} and R_{eq2}, as given in (5.13) and (5.14), were applied in PSpice as a load to a bridge rectifier with dc link capacitor, Figure 5.28. An 'if statement' is implemented in PSpice that monitors the input current to the bridge rectifier, selecting the appropriate load expression (R_{eq1} or R_{eq2}), i.e. if current is greater than zero apply load expression R_{eq2}, else apply load expression R_{eq1}. The variable resistance model is built from a voltage source, while unity value

resistance and current measuring block are built to implement the variable resistor. The value of L_{sys}, (R_{total} = R_{sys} + R_{in}) and C_{dc} were set to be exactly the same as those used in the full 11W CFL model.

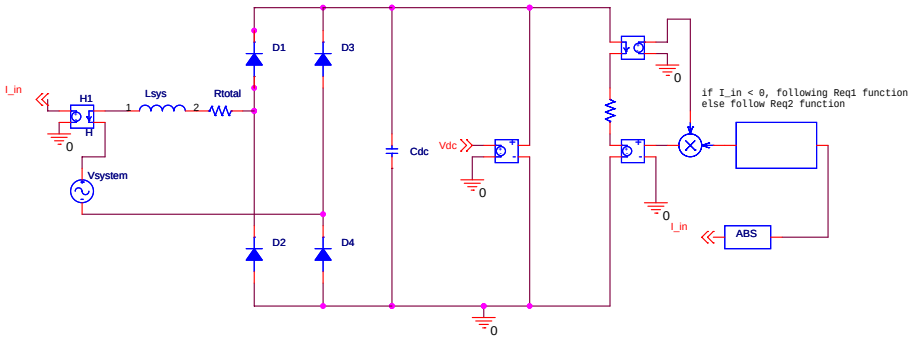
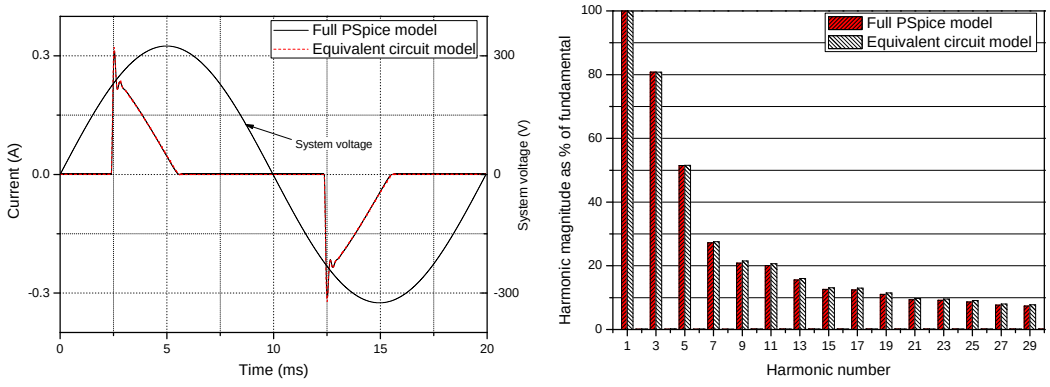


Figure 5.28: *PSpice equivalent circuit of CFL model.*

Simulations were run using the developed equivalent circuit CFL model. Figure 5.29 shows the comparison of the input current waveforms and associated harmonic content between of the full and equivalent circuit models, both supplied with 1pu system voltage. Figure 5.30 shows a comparison between the change in P-V and N-V characteristics of the two models. These comparisons show very clearly that the equivalent circuit model is able to almost exactly predict the input current waveform and harmonic content of the full PSpice CFL model, and also to accurately predict the P-V and N-V characteristics. The small differences in the N-V characteristics are due to the transition periods between the charge and discharge regions being neglected in the equivalent circuit model. The presented results validate the developed equivalent circuit model of the 11W CFL with generic tube. This simple model may now be used instead of full PSpice model, allowing for considerably faster simulation times and to form the basis of analytical model developed in the next section.



(a) Current/voltage waveforms

(b) Current harmonics

Figure 5.29: *Comparison between input current waveforms and associated harmonics of full and equivalent circuit PSpice models of generic CFL, at 1pu system voltage.*

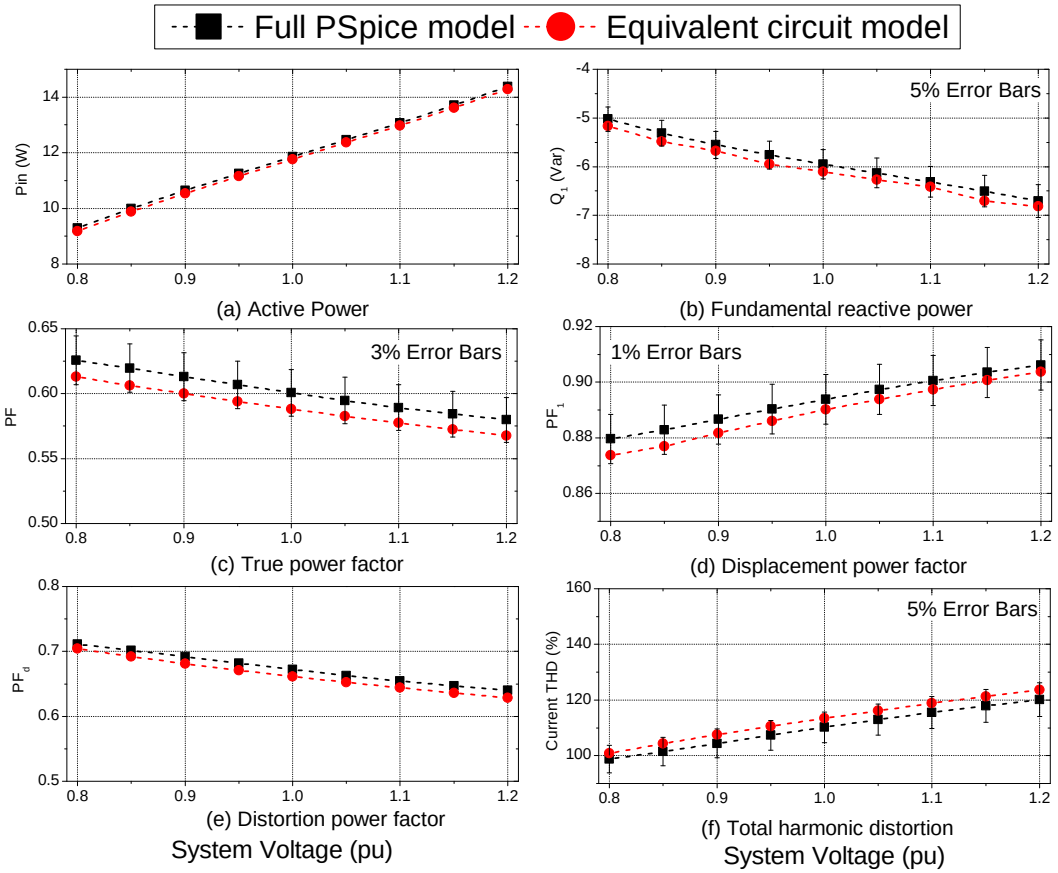


Figure 5.30: *Comparison between P-V and N-V characteristics of full and equivalent circuit PSpice models of generic CFL.*

5.12.3 Per unit representation of equivalent model

So far, developed expressions (5.13) and (5.14) are in absolute form, representing an 11W CFL with generic tube characteristics, Section 5.11.2.1. This is because it was considered easier to derive the equivalent circuit model in absolute form. This absolute form is now converted to per-unit form. All that is required to convert expressions (5.13) and (5.14) into per-unit is a suitable resistance base, given as:

$$R_{b,CFL} = \frac{V^2_{dc(nominal)}}{P_{CFL}} \tag{5.15}$$

where: $V_{dc(nominal)}$ is the average rms dc link voltage when the ballast is supplied with 1pu system voltage and C_{dc} is nominal; P_{CFL} is the rated CFL power, e.g. 11W for a 11W CFL.

In order to use this per-unit system, $V_{dc(nominal)}$ must be known for each of the CFLs with rated active powers between the considered range, 8W - 25W. Thus, $V_{dc(nominal)}$ was investigated

for a range of CFLs, using previously developed models of the 8W, 11W, 15W, 18W, 20W and 25W CFLs. The applied voltage to the models was 1pu system voltage and all ballast component values were set at nominal. The value of $V_{dc(nominal)}$ is plotted as function of CFL rated active power in Figure 5.31. It can be seen that $V_{dc(nominal)}$ is almost constant, ranging from 278V - 282V for considered rated CFL powers. This is because, as previously shown, the value of C_{dc} in the CFLs will be changed in direct proportion the rated power of the CFLs (Figure 5.20 has almost linear relationship for actual C_{dc} versus CFL rated power).

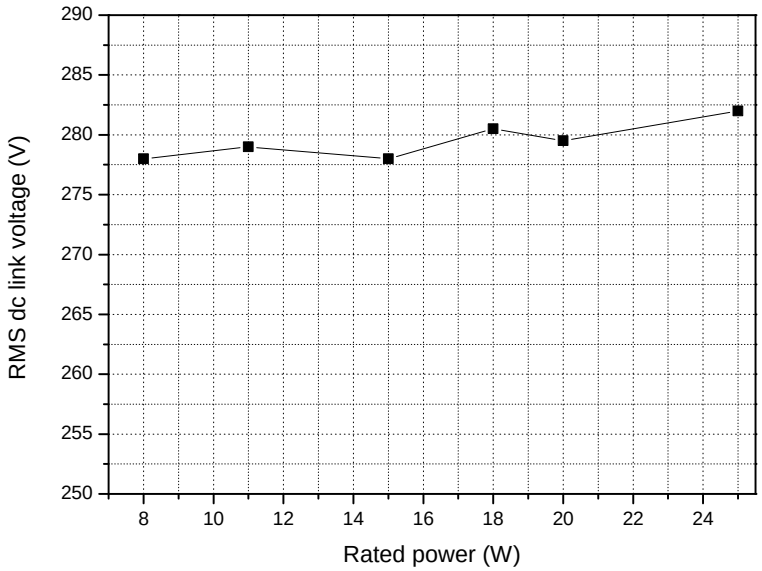


Figure 5.31: *Nominal dc link rms voltage at 1pu system voltage and nominal ballast component values for CFLs at rated powers of 8W, 11W, 15W, 18W, 20W and 25W.*

Therefore, the absolute derived expressions for generic CFL model equivalent resistance (5.13) and (5.14) may be converted to per-unit form using R_{base}, to give:

$$R_{eq1,pu} = \frac{23.7 \cdot v_{dc} + 274}{R_{base}} \tag{5.16}$$

$$R_{eq2,pu} = \frac{11 \cdot v_{dc} + 0.021 \cdot v_{dc}^2 + 1300}{R_{base}} \tag{5.17}$$

The per-unit value of C_{dc} has already been presented in Section 5.10, and this value may be used directly in the per-unit generic model of the CFL. As discussed in Section 5.4.2, CFLs will have a relatively large resistor in the bridge rectifier conduction path. These resistors serve to provide a basic form of inrush current protection. From information obtained after opening CFL ballasts and measuring the value of this input resistor, R_{in}, it was found that typically 8W, 11W and 18W CFLs have resistors of value 9, 10 and 15 Ω respectively. It can be seen that the value of R_{in} is roughly correlated with the rated power of the CFL, and therefore maybe

expressed as a function of rated CFL power, as shown in (5.18).

$$R_{in} = 2.7 + 0.7 * P_{CFL} \tag{5.18}$$

5.13 Generic analytical model of CFL

In line with other work in this thesis, the equivalent circuit model of the 11W CFL with generic tube model should be converted to a generic analytical model of the whole CFL. The analytical model of the single-phase bridge rectifier has been developed and discussed in detail in Section 3.10. By applying per-unit values of C_{dc}, R_{in} and rectifier equivalent resistance expressions, all developed previously, a generic analytical model may be formed. The resulting modified generic analytical model equations are shown in expressions (5.19) to (5.21). These expressions again are implemented in a MatLab script to form the generic analytical CFL model, with this code given in Appendix C.1.2.

Charging:

$$v_{rect} = R_{total} \cdot i_{in} + L_{sys} \cdot \frac{di_{in}}{dt} + v_{dc} \tag{5.19}$$

$$i_{in} = C_{dc} \cdot \frac{dv_{dc}}{dt} + \frac{v_{dc}}{\left(\frac{11 \cdot v_{dc} + 0.021 \cdot v_{dc}^2 + 1300}{R_{b,CFL}}\right)} \tag{5.20}$$

Discharging:

$$v_{dc} = v_{start} \cdot e^{\frac{-t}{\left(\frac{23.7 \cdot v_{dc} + 274}{R_{b,CFL}}\right) \cdot C_{dc}}} \tag{5.21}$$

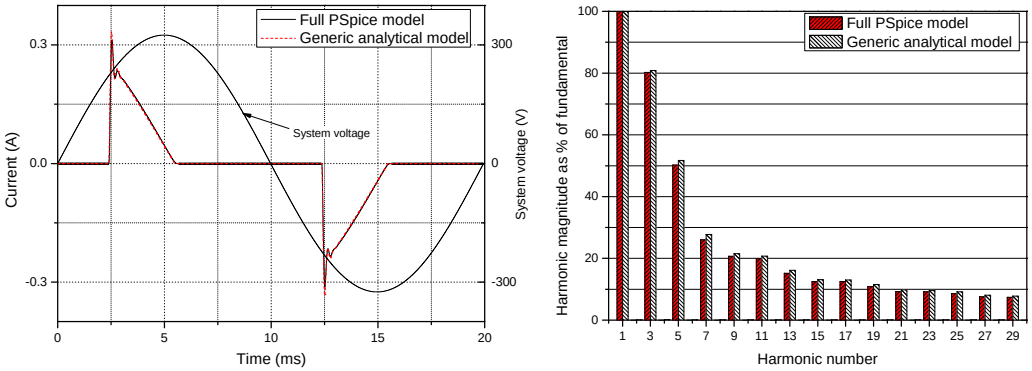
where: i_{in} is the CFL instantaneous input current, v_{rect} is the instantaneous rectified system voltage, v_{dc} and i_{dc} are the instantaneous dc link current and voltage, v_{start} is the capacitor voltage at the start of the discharge period, $R_{b,CFL}$ is defined in (5.15) and R_{total} = R_{sys} + R_{in}.

5.14 Validation of generic analytical CFL model for sinusoidal and non-sinusoidal supply conditions

In order to confirm that the proposed generic analytical CFL model is able to match the power demand and harmonic characteristics of the full PSpice 11W CFL with generic tube model, the two models are compared in this section. Likewise to other chapters, this comparison is performed for both sinusoidal and non-sinusoidal voltage supply conditions. The applied non-sinusoidal supply system waveforms are again “typically” and “heavily” distorted, as

defined in Section 2.12.2. Figures 5.32 and 5.33 show the comparisons of the two models for applied sinusoidal supply voltage. Figures 5.34 and 5.35 show the results of the comparisons for applied "typically distorted" supply voltage and Figures 5.36 and 5.37 show the results of the comparisons for applied "heavily distorted" supply voltage.

5.14.1 Sinusoidal supply conditions



(a) Current/voltage waveforms (b) Current harmonics

Figure 5.32: *Comparison between full model and generic analytical model of 11W CFL with applied 1pu sinusoidal system voltage.*

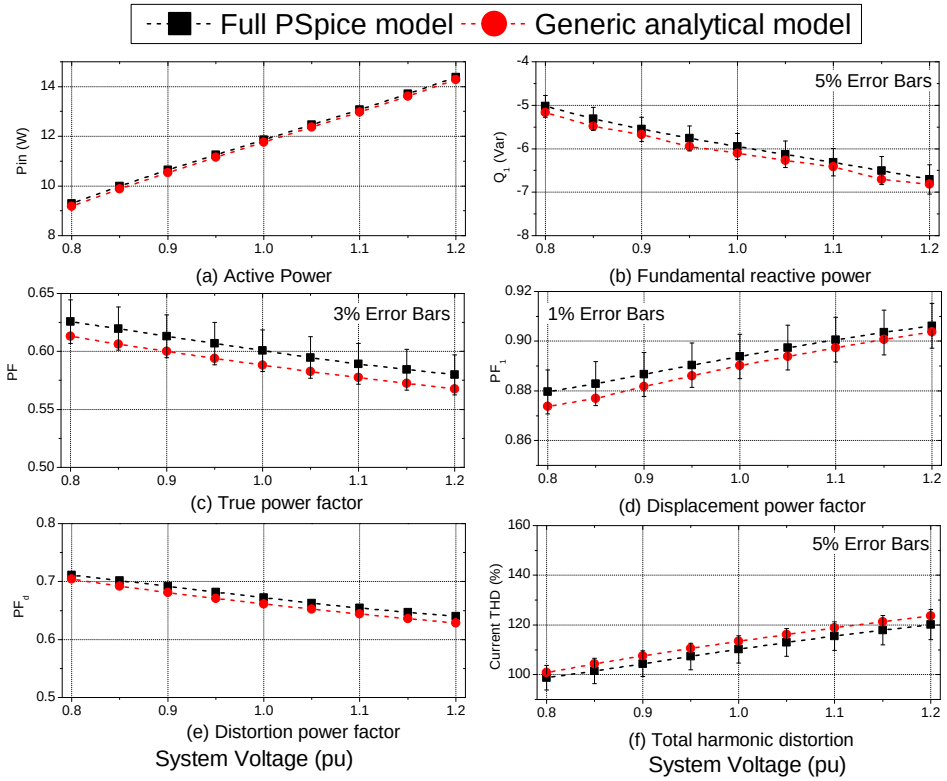
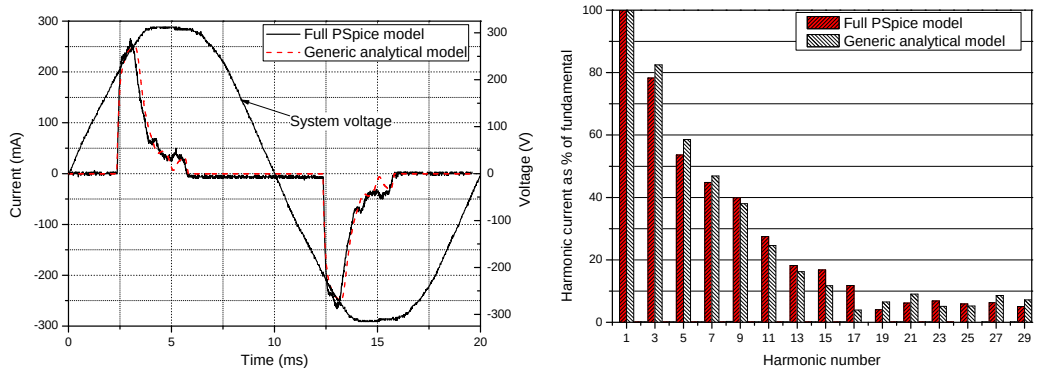


Figure 5.33: *Comparison between power demand characteristics of full model and generic analytical model of 11W CFL with applied sinusoidal system voltage.*

5.14.2 Non-sinusoidal supply conditions, "typically distorted" voltage



(a) Current/voltage waveforms (b) Current harmonics

Figure 5.34: *Comparison between full model and generic analytical model of 11W CFL with applied 1pu "typically distorted" system voltage.*

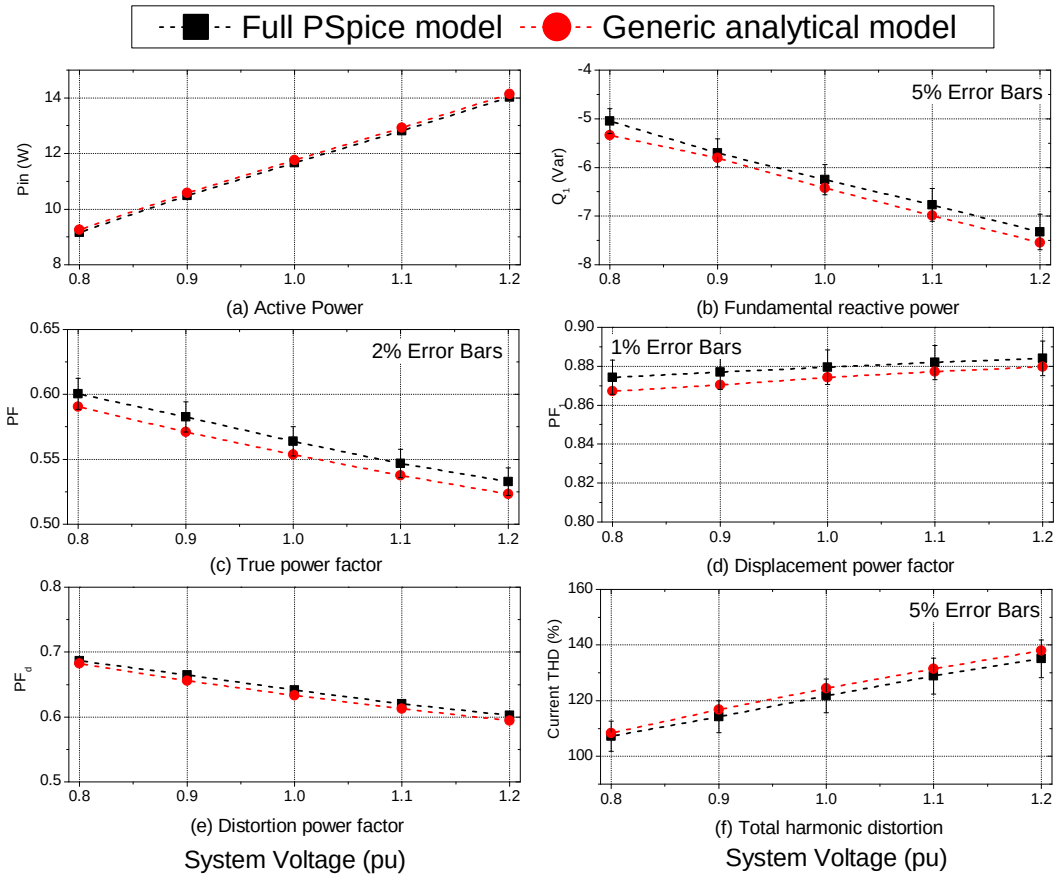
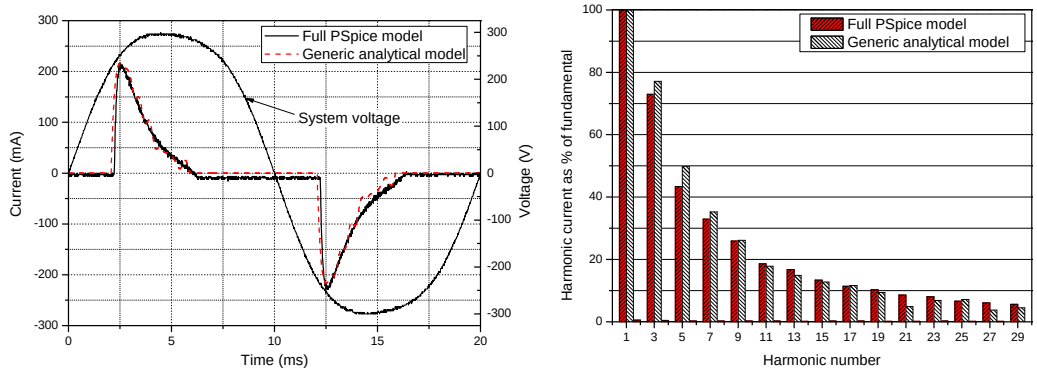


Figure 5.35: *Comparison between power demand characteristics of full model and generic analytical model of 11W CFL with applied "typically distorted" system voltage.*

5.14.3 Non-sinusoidal supply conditions,. "heavily distorted" voltage



(a) Current/voltage waveforms (b) Current harmonics

Figure 5.36: *Comparison between full model and generic analytical model of 11W CFL with applied 1pu "heavily distorted" system voltage.*

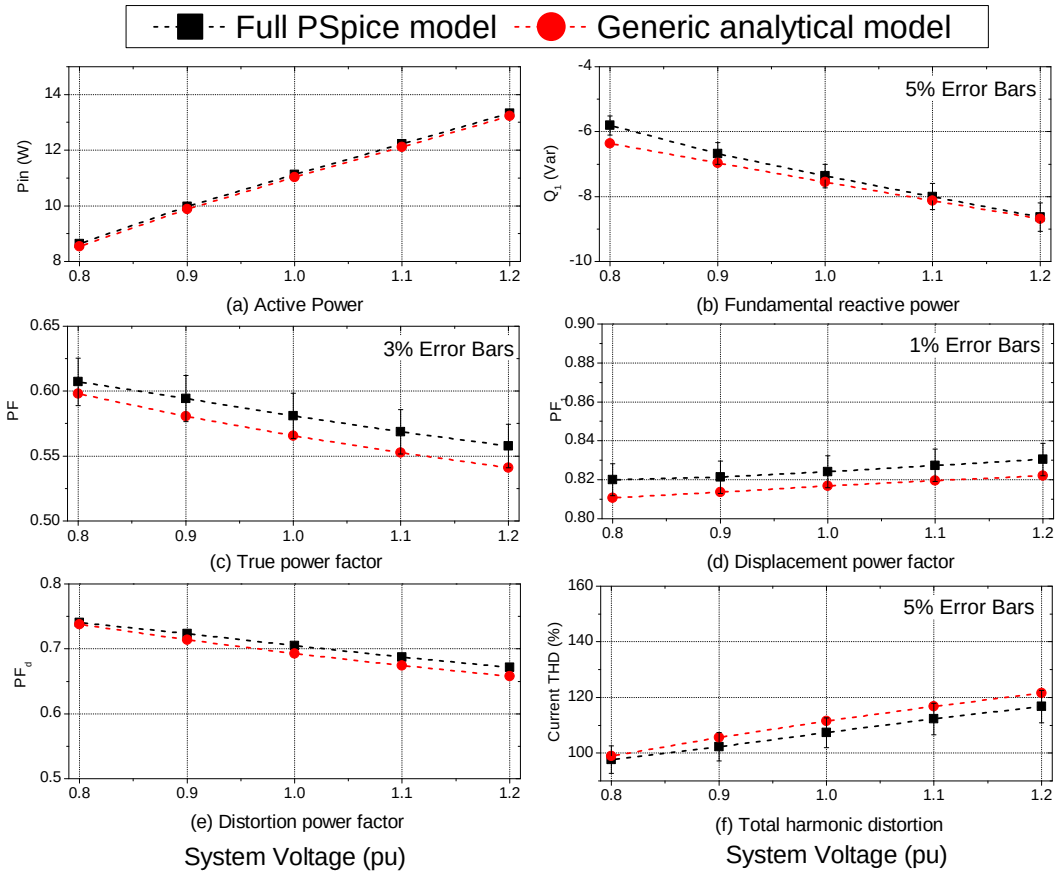


Figure 5.37: *Comparison between power demand characteristics of full model and generic analytical model of 11W CFL with applied "heavily distorted" system voltage.*

5.14.4 Discussion of results

The result of the comparisons shown in Figures 5.32 to 5.37 validate that the generic analytical model is able to represent accurately the shape of the input current waveform of the full PSpice 11W CFL model for all considered sinusoidal and non-sinusoidal supply conditions. Hence, the generic analytical model is also able to accurately represent all power demand characteristics of the full PSpice model for the same sinusoidal and non-sinusoidal supply conditions. This result is to be expected, as the equivalent circuit model of the CFL has been previously validated and the analytical model is a direct representation of this model.

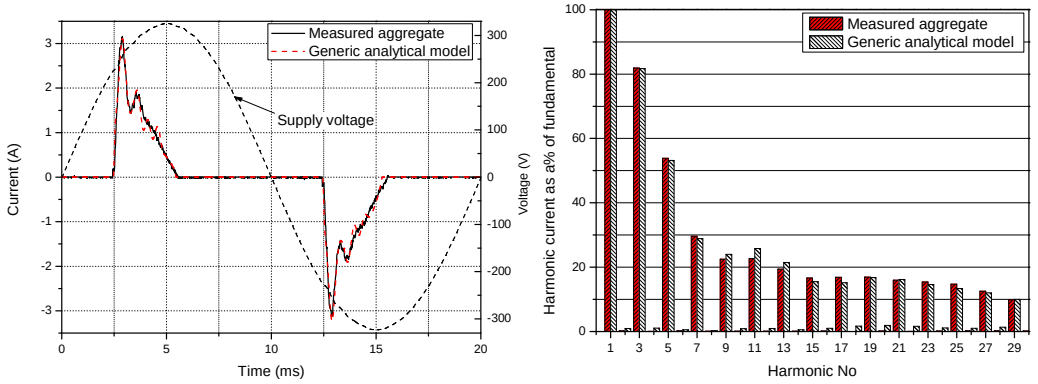
The results of the presented analysis also show that as supply system voltage distortion increases the displacement power factor of the CFL will reduce (as also seen in lower-power SASDs and SMPS with no PFC). This reduction is fairly significant, with PF_1 changing from ≈ 0.89 to ≈ 0.82 between sinusoidal and "heavily distorted" supply conditions. This effect can also be seen in Figures 5.32(a), 5.34(a) and 5.36(a), where the CFL input current waveform will 'shift' to the left and the CFL will become a more capacitive load (see Section 3.12.2). The results further show that harmonic content of the CFL input current does not reduce with increased distortion in the supply system voltage, as has been observed in other non-linear loads considered in this thesis. The presented results in this section therefore validate that the generic analytical model is an accurate representation of the full PSpice model of 11W CFL with generic tube model. The next section validates that the proposed generic analytical model can be used to represent the power demand characteristics and harmonic properties of a same-type aggregate of CFL loads with different rated powers.

5.15 Verification of proposed generic analytical CFL model with measurements of aggregate CFL load

This section compares the characteristics of a measured aggregate CFL load with characteristics predicted by the proposed generic analytical CFL model. As the generic tube model, which dictates the P-V characteristics of the CFL, was itself derived from the average per-unit P-V characteristics of several CFLs (see Section 5.11.2.1), the generic analytical model should be well suited for representing an aggregate of CFLs. The ballast circuit is also a generic circuit, as the self-oscillating topology is dominant in CFLs. Finally, the value of C_{dc} in CFLs can be very well defined, as harmonic legislation provides an upper limit for its size and tube lifetime considerations (tube crest factor) provide a clear lower limit for its size. The difference between these two limits is relatively small, and therefore the value of C_{dc} in a particular CFL will not show much variance from typical expected value, i.e. per-unit value of C_{dc}.

As discussed in Section 5.2.2, the most common types of GILs used in domestic applications are

of rated power 40W, 60W and 100W, respectively making up 20%, 50% and 20% of currently estimated domestic lighting load, [96]. These GILs are expected to be replaced by 8W, 11W and 18W CFLs, as they give similar output lumens. Thus, the measured aggregate load was made up of roughly 22% 8W CFLs, 56% 11W CFLs and 22% 18W CFLs, in order to form a typical CFL aggregate load. A controllable voltage source, [92], was used to supply sinusoidal voltage to this aggregate load, with this voltage altered between 0.8-1.2pu of nominal system voltage. At each voltage, the current waveform of the aggregate load was measured and used along with the system voltage waveform to calculated the power demanded from the voltage source by the aggregate load. The generic analytical model was set to the rated power of the aggregate load. As the measured aggregate load actually distorted the voltage waveform supplied by the controllable voltage source, this distorted voltage was measured and reconstructed to supply the generic aggregate model, in order for a fair comparison of model and measurement to be made. Figures 5.38 and 5.39 show the comparisons of measured aggregate CFL load and corresponding generic analytical model.



(a) Current/voltage waveforms (b) Current harmonics

Figure 5.38: *Comparison between measured aggregate CFL load and corresponding generic analytical CFL model, for applied 1pu sinusoidal voltage.*

Figure 5.39(a) demonstrates that the generic analytical model can very accurately predict the P-V characteristics of the measured aggregate load. Therefore, this result provides complete validation of the proposed generic tube model, as the tube will dictate active power demand characteristics. There is a small error between predicted and measured Q_1-V characteristics, with maximum error of only 4% at the end of considered range for system voltage. Furthermore, the results presented in Figure 5.38 show a very good matching of generic analytical model input current waveform with the measured results. Accordingly, the generic analytical model is able to predict the harmonic characteristics of the measured aggregate load without any significant error. It can also be seen from Figures 5.39(e) and (f) that the generic analytical model can maintain this accurate representation of measured aggregate load harmonic characteristics for the full range of considered system voltage.

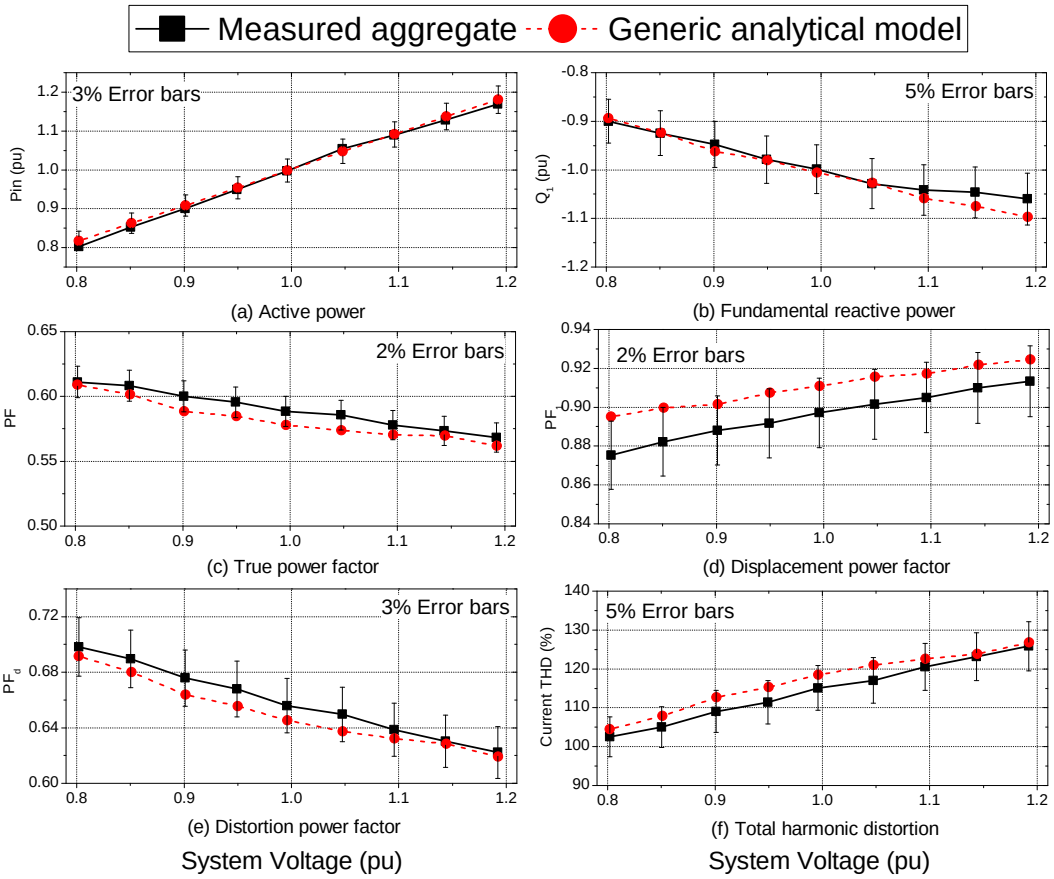


Figure 5.39: *Comparison between power demand characteristics of measured aggregate CFL load and corresponding generic analytical CFL model, with applied sinusoidal system voltage.*

This exceptionally good matching between measured aggregate load and analytical CFL model is achieved as the generic tube model was constructed based on measured data and will therefore have the average P-V characteristics of 8W, 11W and 18W CFLs. Accordingly, the proposed generic CFL model is ideally suited to represent the P-V characteristics of an aggregation of CFLs. The results also further confirm that the per-unit values of C_{dc} and R_{in} are indeed representative of the typical values of these components in CFL loads. Therefore, the proposed generic analytical model of CFL may be used directly to represent the steady state operating characteristics of an aggregation of CFL loads.

5.16 Polynomial and exponential models of CFLs and LFLs

To complete the analysis of the CFL load type, polynomial and exponential interpretations of the proposed generic analytical model are now presented. In the same way as in other chapters in this thesis, the polynomial and exponential models are found by fitting associated model

coefficients to the P-V and Q_1-V characteristics shown in Figure 5.39. The resulting model coefficients are shown in Table5.4. It should be noted that as CFL is a capacitive load, the fundamental reactive power coefficients of the polynomial model will sum to -1. There is no such mechanism for the representation of capacitive loads in the exponential model.

As discussed in Section 5.11, modern LFLs are expected to include active PFC in order to meet harmonic legislation. Therefore, modern LFL load will draw constant active power, independent of changes in system voltage, and will operate with unity value of true power factor. The polynomial and exponential models of LFLs are also shown in Table 5.4. Comparison of the proposed polynomial and exponential models with existing models of CFLs and LFLs (Table 5.1) are shown in Figure 5.40. A comparison of the 'goodness of fit' of the proposed models to the original data is not presented in Figure 5.40, as the P-V and Q_1-V power demand characteristics of CFLs are linear, and can be very well represented by both polynomial and exponential models.

Table 5.4: *Proposed, polynomial and exponential model coefficients of CFL and LFL load.*

PF_1	Exp. Model		Polynomial model					
	np	nq	Z_p	I_p	P_p	Z_q	I_q	P_q
Compact fluorescent lamps (CFL)								
0.91	0.94	0.52	-0.01	0.96	0.05	0.10	-0.73	-0.37
Linear fluorescent lamps (LFL)								
1.00	-	0	0	0	1	-	-	-

The comparisons in Figure 5.40 show that there is a fairly good agreement between proposed and existing models of CFLs for both P-V and Q_1-V power demand characteristics. However, only one of the existing models, Model 3, presents a value for displacement power factor for CFL, which is in disagreement with the proposed value. These comparisons are interesting, as they indicate that modern CFLs will have similar P-V and Q_1-V demand characteristics to older CFLs, (most likely because of similar fluorescent tubes used in both modern and older CFLs), although due to the introduction of harmonic legislation these loads will now operate at reduced displacement power factors.

The effect of harmonic legislation can most clearly be seen when comparing proposed and existing model P-V and Q_1-V power demand characteristics of LFLs. It can be seen that LFLs are now expected to have constant P-V characteristics with no fundamental reactive power component, which is a direct result of harmonic legislation. Although Model 1 does predict these characteristics of LFLs, this model was developed in 1992 and is also suspected to be a somewhat arbitrary model. However, ironically, Model 1 is now more valid than the other subsequently proposed models of LFLs.

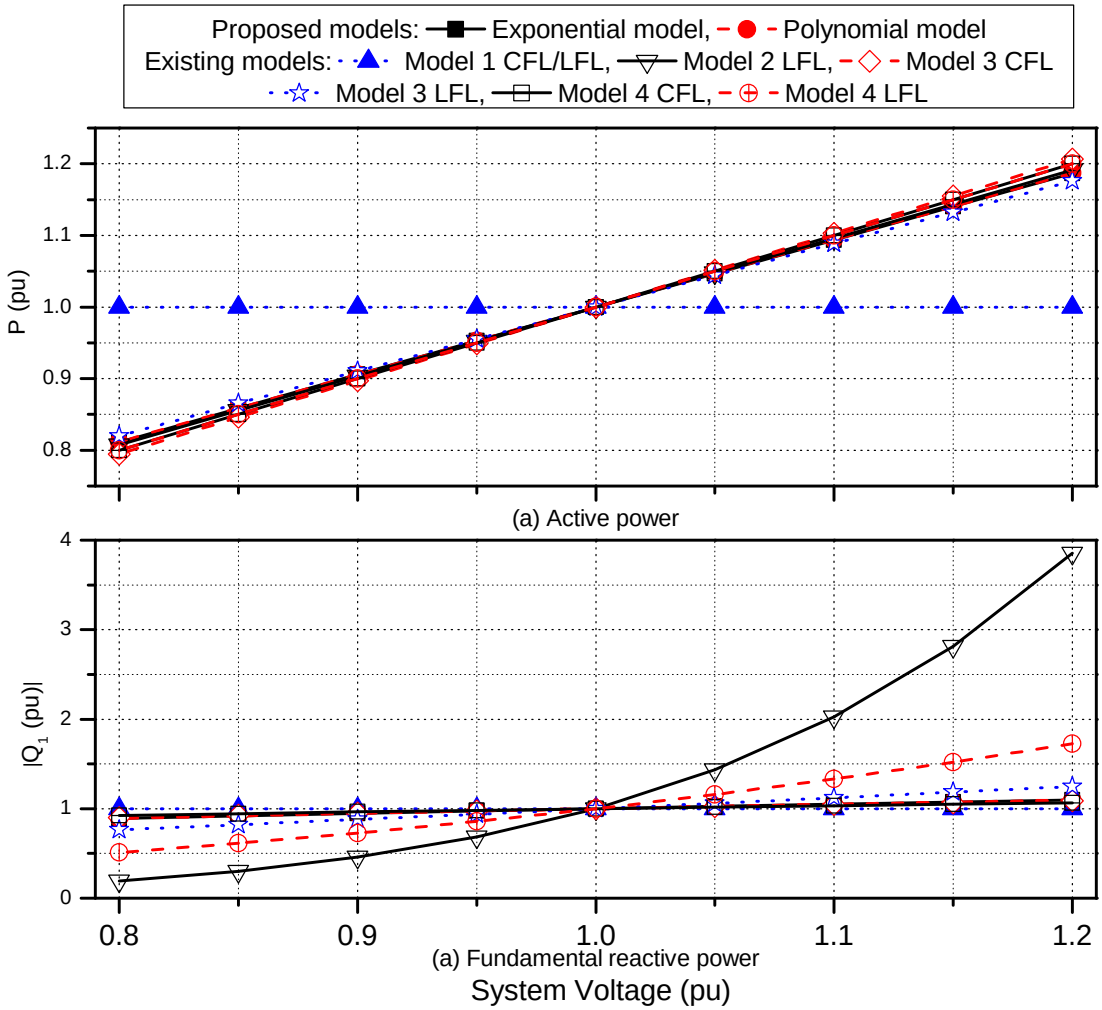


Figure 5.40: *Comparison between proposed CFL models and existing models found in literature.*

5.17 Conclusions

This chapter has considered existing and future UK lighting load, identifying how the present load mix is likely to change significantly over the next few years/decades. The major changes will be related to the replacement of traditional incandescent light sources with low-energy consumption light sources, specifically CFL in the domestic/residential load sector. These loads have considerably different characteristics to traditional incandescent lighting, and, clearly, there is a need to develop new load models.

It is shown that there are two common types of electronic ballast circuits used in CFLs and LFLs: self-oscillating ballast, which is used almost exclusively in CFLs, and the IC-controlled ballast, which is used mainly in LFLs. A review of previous work on the representation of fluorescent tubes is also performed, with the conclusions that there has been little work on the representation of tubes in modern CFLs. In order to obtain a correct tube model, measurements

were performed on a range of typical CFLs, and a new tube model, developed from these measurements, is presented. The tube model is incorporated with a detailed ballast model in PSpice, forming a full CFL model, which is validated using the measured data.

The harmonic legislative requirements that CFLs must comply with have also been considered, showing that they are the driving force behind the design of modern CFLs and LFLs. Based on these harmonic limits, CFLs and LFLs are divided into those with rated active power less than and above 25W. In practice, all CFLs will have rated power less than 25W, and the vast majority of LFLs will operate at powers greater than 25W. Due to these harmonic limits, LFLs will include active power factor correction circuitry. This makes them to appear as constant active power loads, drawing no reactive power from the supply. CFLs, however, cannot be represented in such a simple way, as they can meet harmonic legislation without large and more costly active PFC circuits.

The characteristics of CFLs are dominantly influenced by dc link capacitance, which, in turn, is determined as a trade-off in satisfying requirements for harmonic emission and expected lifetime. The characteristics of a range of typical CFLs, obtained from measurements, were used to develop a generic CFL model. As this model is not suitable for representing aggregate CFL loads, an equivalent resistance CFL model was developed. This equivalent resistance model was then converted to an analytical CFL model, allowing to significantly reduce simulation times. The generic analytical CFL model was used for modelling aggregated CFL load, and also validated against measured data. The developed model was in very good agreement with measurements. Exponential and polynomial interpretations of proposed generic CFL and LFLs models were also given in this chapter.

Finally, comparisons were made between the developed and existing load models of CFLs and LFLs. These comparisons showed good agreement between active and fundamental reactive power characteristics for the majority of considered existing CFL models. However, there was a disagreement in the prediction of displacement power factor. This is a direct result of harmonic legislation, which was not mandatory when previous CFL models were developed. Similar conclusions are drawn when comparing proposed LFL models to previous models, where modern LFLs are shown to have considerably different characteristics to the previous ones. It is also shown that previous load models cannot be used for any form of harmonic analysis, and therefore their usefulness for the prediction of the characteristics of modern lighting loads is limited.

Chapter 6
Modelling of aggregate loads

6.1 Introduction

Generic analytical models of common types and sub-types of loads have been developed and validated in previous chapters. Additionally, polynomial and exponential interpretations have been derived from these generic analytical models. This chapter aims to illustrate some of the possible applications of the developed models, highlighting their flexibility and versatility. This is achieved by aggregating developed load models to represent typical present and future load mixes established from a review of available statistics and predictions/estimations for the future.

The P-V and Q_1-V characteristics of present and predicted future aggregate loads are investigated, where it is shown that there is significant difference between load characteristics predicted by aggregate load formed from proposed and previously proposed (existing) individual load models. It is also shown that system voltage distortion will affect aggregate load displacement power factor, and hence aggregate load fundamental reactive power demand. Aggregate loads are then applied to a typical UK/Scotland distribution network, and network load meeting capacity (LMC) is investigated with the considered different aggregate loads. It is shown that different aggregate loads will have significantly different effects on the LMC of the considered typical network, which additionally highlights the importance of accurate load models in power system studies.

To further illustrate the comprehensive nature of developed models, they are also used to investigate the harmonic characteristics of the present and future load mixes. It is shown that the proposed aggregate load models are able to correctly represent the harmonic interactions between different types and sub-types of considered loads. A simple two-bus representation of a domestic feeder is then used to investigate some of the effects of increased number of non-linear loads in the future on the supplies system, specifically the effect on supply bus voltage distortion. It is found that the voltage distortion of a typical load bus is expected to increase by around 30% (from the present value) for future load.

One of the possible ways to present analysis in this chapter is to perform extensive detailed power system analysis using the developed load models. However, the majority of time available for this PhD research was allocated to the development of presented load models and

detailed analysis using the developed load models should be subject of future research based on the presented PhD thesis results. This is further considered in Section 7.2 where future work is discussed.

6.2 Aggregation of developed load models

The methods used to aggregate the polynomial, exponential and analytical load models developed in this thesis are presented in this section.

6.2.1 Aggregation of polynomial and exponential load models

6.2.1.1 Aggregation of polynomial load models

The standard approach to the aggregation of polynomial models of individual load type/sub-type is described in [13], [22], [112] and [113]. This approach uses the percentage bus load composition of each load types/sub-types to calculate a weighted average of each polynomial model coefficient. This method is used for the aggregation of the individual (device-based) polynomial models developed in this thesis, and is described by (6.1) and (6.2).

$$A_P = \sum_{n=1}^{N} (c_n \cdot a_n)/100 \tag{6.1}$$

$$A_Q = \sum_{n=1}^{N} (\tan(\cos^{-1}(PF_{1,n}))/100 \cdot c_n \cdot a_n) \tag{6.2}$$

Where: N is the total number of different load types in the aggregate load mix, n is the particular load type, c_n is the percentage contribution of load type n, a_n is the load type coefficient either $Z_{p/q}$, $I_{p/q}$ or $P_{p/q}$ for load type n, A_P and A_Q are the aggregate load coefficients $Z_{p/q}$, $I_{p/q}$, $P_{p/q}$ and $PF_{1,n}$ is the displacement power factor of load type n.

If the considered individual load type is capacitive, the corresponding load type coefficients Z_q, I_q and P_q (represented by a_n) will sum to -1, if inductive to +1, and if resistive to zero. Therefore, if the aggregate load is formed from a mix of capacitive, inductive and resistive loads, negative displacement power factor values for capacitive loads will be summed algebraically with the positive power factor values for inductive loads, giving correct aggregation displacement power factor.

Expressions (6.3) to (6.4) present the aggregate bus load models in polynomial form. The

displacement power factor of each load type is incorporated directly into the polynomial coefficient of reactive power as shown in (6.2). In this way, absolute aggregate fundamental reactive power demand may be expressed in terms of the nominal active power demand, as in (6.4). This helps to make the aggregate load models more accessible, as the information about nominal active power demand at a particular system bus is normally more readily available than the information about bus nominal fundamental reactive power demand.

$$P_{agg,polynomial} = P_0 \cdot \left[Z_p \cdot \left(\frac{V_{bus}}{V_{nom}} \right)^2 + I_p \cdot \left(\frac{V_{bus}}{V_{nom}} \right) + P_p \right] \tag{6.3}$$

$$Q_{agg,polynomial} = P_0 \cdot \left[Z_q \cdot \left(\frac{V_{bus}}{V_{nom}} \right)^2 + I_q \cdot \left(\frac{V_{bus}}{V_{nom}} \right) + P_q \right] \tag{6.4}$$

Where: $P_{agg,polynmial}$ and $Q_{agg,polynmial}$ are the aggregate active and fundamental reactive power demands at the considered bus, respectively, P_0 is the nominal bus active power demand, V_{bus} is actual bus voltage and V_{nom} is the nominal bus voltage.

6.2.1.2 Aggregation of exponential load models

The method of aggregation of the exponential model is not considered in [13], [22], [112], or [113]. This is because aggregation of the individual load fundamental reactive power characteristics can not be performed in a direct way, as the structure of the exponential model is, $Q_{1,pu} = P_0 \cdot \tan(\cos^{-1}(PF_1)) \cdot (V_{pu})^{nq}$, (where $P_0 \cdot \tan(\cos^{-1}(PF_1))$ represents nominal fundamental reactive power demand). If the aggregate exponential model is to be formed from a mixture of capacitive, inductive and resistive loads, nq cannot be set to represent zero or negative fundamental reactive power. Therefore, the only way in which aggregation of fundamental reactive power may be achieved is to calculate the value of fundamental reactive power associated with each load separately and then sum these numerical values to find the numerical aggregate. This can be performed at a range of system voltages to produce the aggregate load Q_1-V characteristic. An exponential model then may be re-fitted to this characteristic, to find the aggregate load coefficient, nq. In order for this method to work, an additional coefficient should be included, as shown in (6.5). This additional coefficient can be used to determine whether the considered load type is inductive, capacitive or resistive.

$$Q_{1,pu} = a_q \cdot \left[\tan(\cos^{-1}(PF_1)) \cdot (V_{pu})^{nq} \right] \tag{6.5}$$

Where: $a_q = 1$ load type is inductive, $a_q = 0$ load type is resistive and $a_q = -1$ load type is capacitive.

6.2.2 Aggregation of analytical models

The developed generic analytical load models of each load type and sub-type considered in this thesis are aggregated in this chapter. Similarly to the aggregation of exponential and polynomial load representations, the percentage contribution of each load type/sub-type in the aggregate load (i.e. in the load mix) is required to form the aggregate load. However, in addition, information about instantaneous system voltage waveform and the system impedance is required (Note: In exponential and polynomial models, the system voltage is implicity assumed to be sinusoidal, as these loads models do not consider the effect of non-sinusoidal supply voltages on load characteristics). It has been shown, in previous chapters that system impedance will have little to no effect when varied between minimum, nominal and maximum expected typical values for load types that include active and passive PFC. Although, the value of system impedance will have more effect on load types that do not include PFC, these loads tend to operate at high displacement power factors, so effects on fundamental reactive power will again be small.

Therefore, the input parameters to each individual generic analytical model are the instantaneous system voltage, the system impedance and the percentage contribution of the particular load type/sub-type to total/aggregate load. Each model is then solved to find its associated instantaneous current waveform. These current waveforms then may be summed, to give the instantaneous current waveform of the non-linear aggregate load. Linear loads may be represented as a sinusoidal current waveforms, with phase shift and magnitude dependent on their power factors and percentage contributions to the aggregate load. Non-linear and linear aggregate current waveforms may then, finally, be summed, to give the instantaneous current waveform of the aggregate load. Figure 6.1 shows this aggregation procedure. A MatLab code was developed to implement the aggregation procedure, and this code can be found in Appendix D.1.

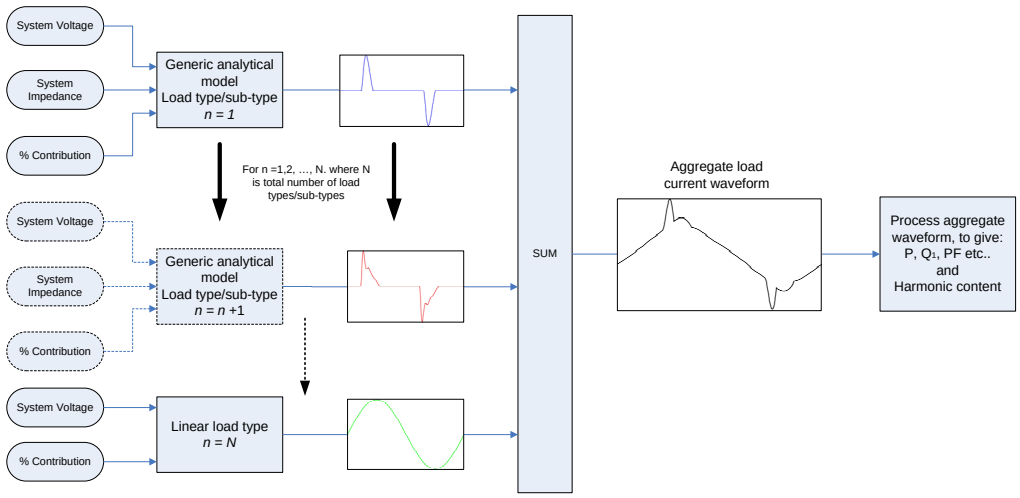


Figure 6.1: *Flow diagram of aggregation procedure for generic analytical models and linear loads.*

The instantaneous current waveform of the aggregate load are then processed, together with the instant system voltage waveform, to find all required power demand quantities and indicators, i.e. P, Q_1, PF, THD etc. The magnitude of the system voltage may be altered to find the P-V and N-V demand characteristics of the aggregate load. Polynomial and/or exponential expressions may then be fit to the resulting P-V and Q_1-V characteristics, to produce polynomial and exponential interpretations of the aggregate load that can be used directly in standard load flow analysis. However, all other information about aggregate load will be lost, i.e. harmonic content.

6.2.3 Comparison of aggregate loads from developed models with measurements

Initial measurements were performed on a made-up aggregate load, which consisted of 30% SMPS' with no PFC, 10% CFLs and 60% resistive load. This aggregate load was constructed to roughly model an aggregate domestic load, where the resistive load represents linear loads such as motors and heating, the SMPS represents electronic loads, and, of course, the CFLs representing lighting load. This aggregate load was initially supplied with a sinusoidal voltage produced by a linear power supply, [90]. The magnitude of sinusoidal voltage was varied in range between 0.8 and 1.2pu of nominal, in steps of 0.1 pu voltage, with the aggregate load allowed to reach steady state between each change in voltage. The aggregate current waveform was recorded at each voltage, with Figure 6.2 showing this composite/aggregate current waveform and associated harmonics at 1pu system voltage. From the measured current and applied voltage waveforms, the P-V and N-V characteristics of the aggregate load were also found and shown in Figure 6.3.

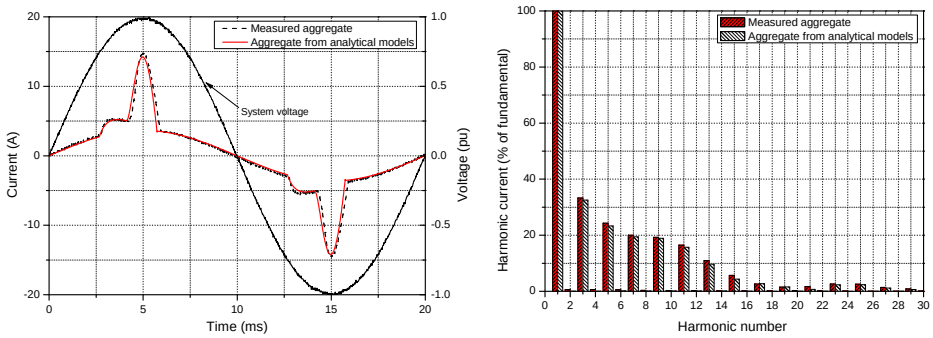
The individual polynomial and exponential models of the SMPS, CFL and resistive load developed in this thesis were aggregated (see Section 6.2) in the correct percentage contribution, so as to represent the measured aggregate load. Accordingly, the P-V, Q_1-V and PF_1-V characteristics of aggregate load models are also shown in Figure 6.3. The characteristics of the aggregate load predicted by both polynomial and exponential models are essentially identical, and they are presented using a single line in Figure 6.3. This matching of polynomial and exponential aggregate models is to be expected, as from Sections 5.16 and 4.9 it can be seen that both CFL and SMPS can be equally well modelled with either polynomial or exponential models, due to the general linear shape of their P-V and Q_1-V characteristics.

The generic analytical models of the SMPS with no PFC and CFL were also aggregated, using the load mix data of the measured aggregate load. An ideal sinusoidal system voltage waveform was applied to the models. Figure 6.2 shows the predicted current waveform and associated current harmonics of the aggregated analytical load, with Figure 6.3 showing the associated P-V and N-V characteristics.

Further to applying sinusoidal voltage to the measured aggregated load, the controllable ac

power source was also programmed to reproduce and apply the "typically" and "heavily" distorted system voltages, as described in Section 2.12.2. Again, voltage sweeps were performed to obtain the P-V and N-V characteristics of this measured aggregate load when operating under non-sinusoidal conditions. The results of this analysis are shown in Figures 6.4 to 6.7, illustrating the current waveforms, current harmonics and power demand characteristics of the analytical aggregated model with applied distorted system voltage waveforms. The aggregate polynomial and exponential loads are as well shown in Figures 6.5 and 6.7, although these models cannot take system voltage distortion into account. Finally, the "typically" and "heavily" distorted system voltage waveforms were also applied to the generic analytical models, which were then aggregated. The result of these analysis are as well shown in Figures 6.4 to 6.7.

6.2.3.1 Sinusoidal voltage supply conditions



(a) Current/voltage waveforms (b) Current harmonics

Figure 6.2: *Comparison of current waveforms and associated harmonics of measured and modelled aggregate load under sinusoidal voltage supply conditions.*

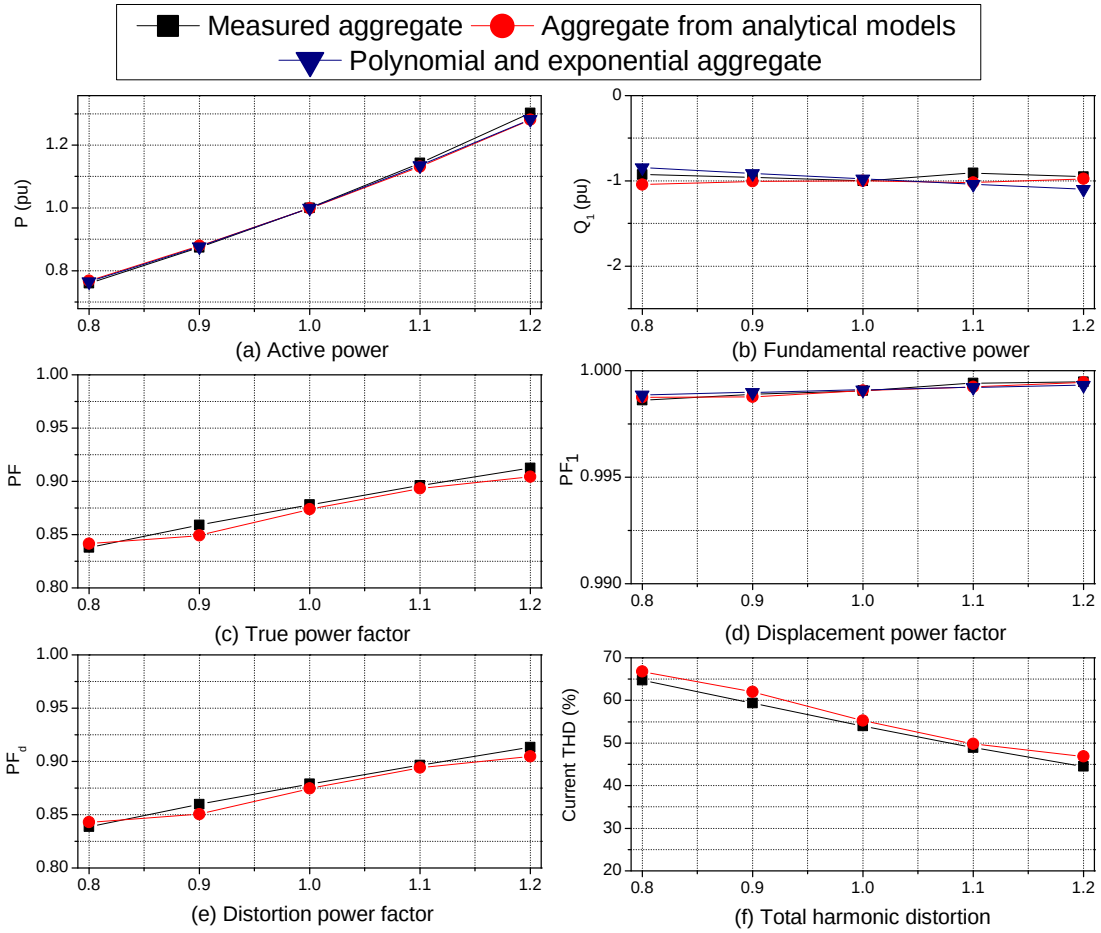
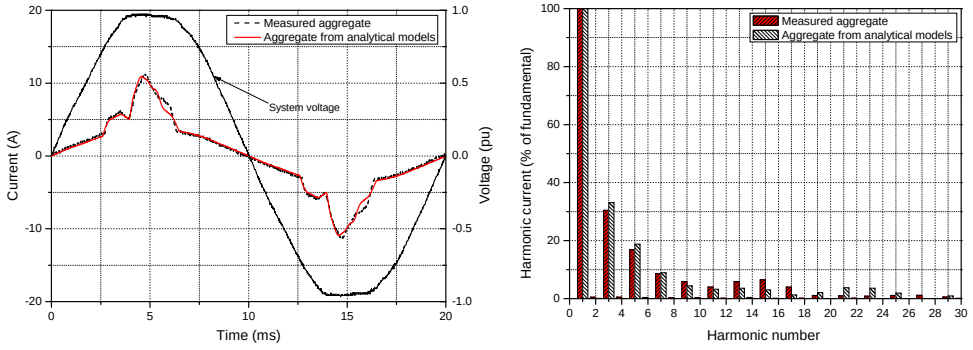


Figure 6.3: *Comparison of active and non-active power demand characteristics of measured and modelled aggregate load under sinusoidal supply conditions.*

6.2.3.2 "Typically distorted" voltage supply conditions



(a) Waveforms (b) Harmonics

Figure 6.4: *Comparison of current waveforms and associated harmonics of measured and modelled aggregate load under "typically distorted" voltage supply conditions.*

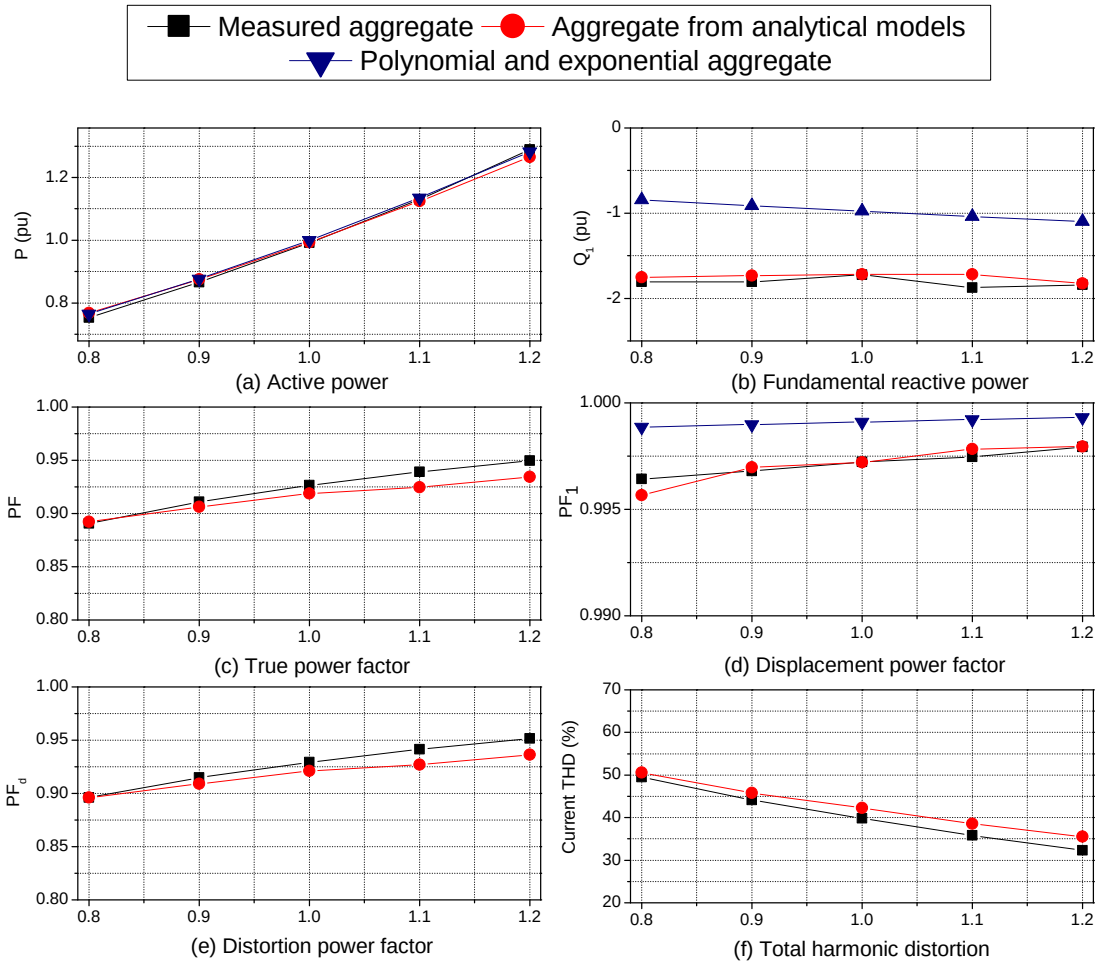
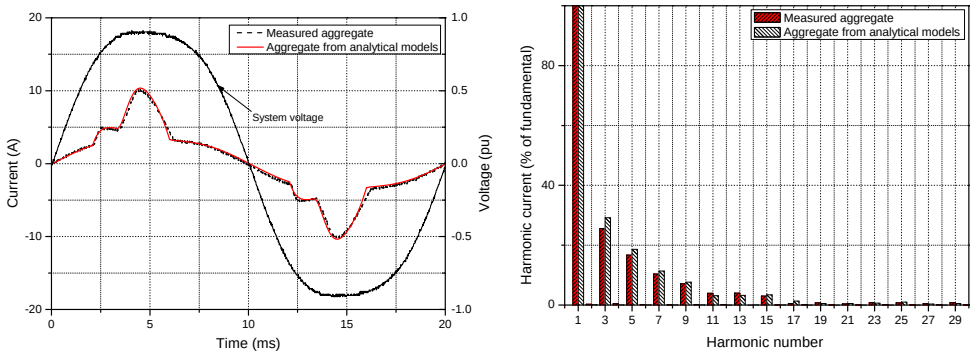


Figure 6.5: *Comparison of active and non-active power demand characteristics of measured and modelled aggregate load under "typically distorted" voltage supply conditions.*

6.2.3.3 "Heavily distorted" voltage supply conditions



(a) Waveforms (b) Harmonics

Figure 6.6: *Comparison of current waveforms and associated harmonics of measured and modelled aggregate load under "heavily distorted" voltage supply conditions.*

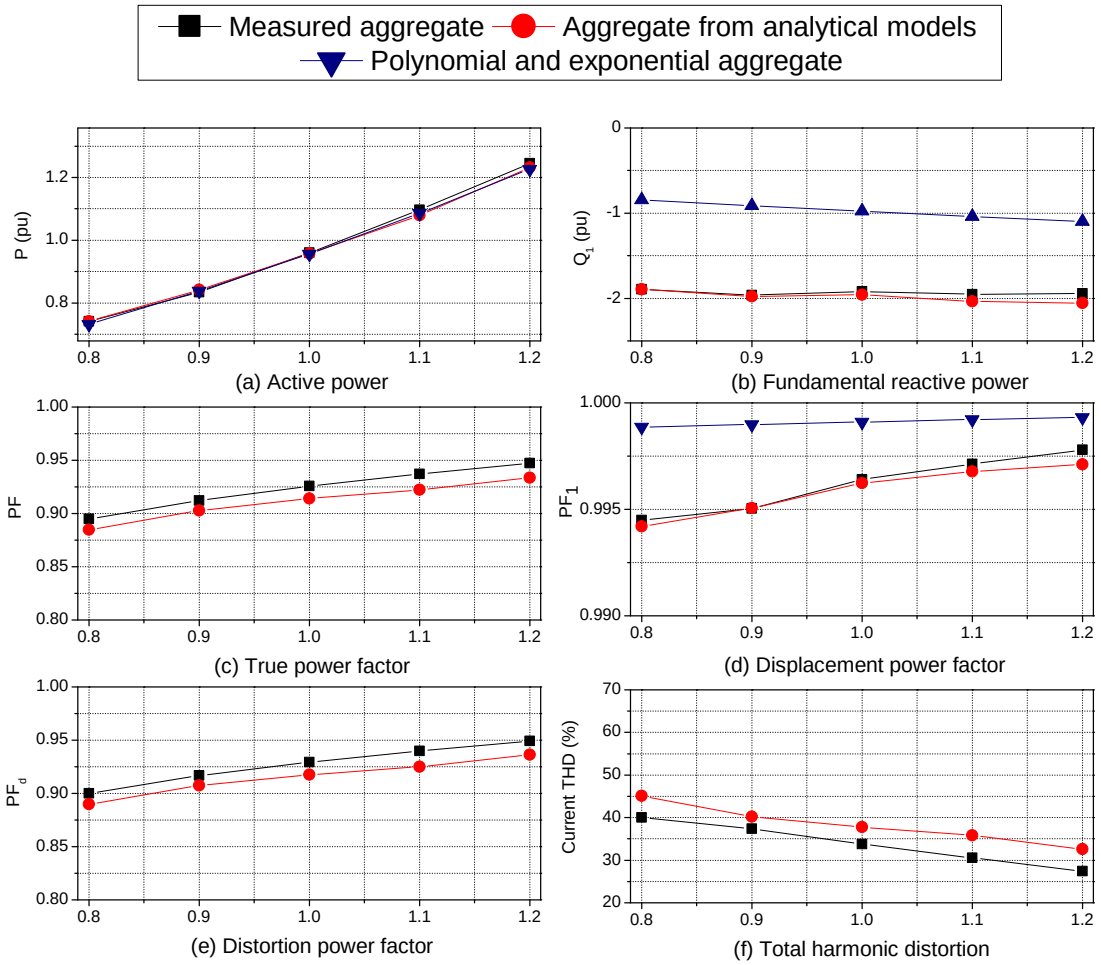


Figure 6.7: *Comparison of active and non-active power demand characteristics of measured and modelled aggregate load under "heavily distorted" voltage supply conditions.*

6.2.4 Discussion of results

It can be seen from the results presented in Figure 6.2 that the analytical model (i.e. the aggregate load formed from individual analytical models) is able to very accurately predict the actual current waveform of the measured aggregate load. As all harmonics and power indicators are derived directly from the current waveform, the analytical model is able to predict these values accurately at 1.0 per-unit system voltage, as can be seen in Figure 6.3. For other values of system voltage, it can be seen from Figure 6.3 that the analytical model continues to predict active and non-active power characteristics of the measured aggregate load with no significant error. The polynomial and exponential models also show good matching of P-V, Q_1-V and PF_1-V to measured results for sinusoidal supply conditions. It should also be noted that the aggregate load is capacitive as both the CFL and SMPS with no PFC are capacitive loads.

When considering the characteristics of measured and modelled aggregate loads with applied

"typically distorted" system voltage, Figures 6.4 and 6.5, it can be seen again that the analytical model is able to predict the current waveform of the measured aggregate with a high degree of accuracy. There is also no significant error in the prediction of active and non-active power demand characteristics with the changes in system voltage magnitude between the analytical and measured aggregate loads. However, the polynomial and exponential models are able to accurately predict only the P-V characteristics of the measured results, but are unable to accurately predict Q_1-V and, accordingly, PF_1-V characteristics. This is because the nominal displacement power factor of the measured aggregate load has altered from 0.999 under sinusoidal conditions to 0.997 under typically distorted system voltage. This very slight change in power factor has a large effect on the nominal value of Q_1, although PF_1 is very close to unity in both cases.

The results presented in Figures 6.6 and 6.7, for "heavily distorted" system voltage show once more that the aggregate load formed from individual analytical models is able to predict measured result even under these extreme conditions, with no significant error between measured and predicted current waveforms and active and non-active power demand characteristics. The nominal PF_1 of the aggregate load has further decreased from 0.997 with "typically distorted" system voltage to 0.996. Again, this slight change has a large effect on nominal value of Q_1.

The results of the initial analysis with the proposed aggregate load formed from individual analytical models has shown that it is able to predict all relevant characteristics of the actual aggregate load for variations in system voltage magnitude and harmonic distortion. This is expected, as the aggregated analytical load is built from individual generic analytical models, which have been validated in preceding chapters of this thesis. The polynomial and exponential load models have been shown to be able to predict only active power demand characteristics of the aggregate load without significant error for all considered supply system harmonic and voltage variations. It has been shown, however, that changes in non-active power demand characteristics due to distortion of the supply system voltage can not be represented with polynmial/exponential models. The next sections will quantify the overall effect of this model deficiency when more realistic system bus load mixes are aggregated.

6.3 Present and expected future typical aggregate load mixes

In order to apply the load models developed in this thesis for the investigation of characteristics of present and future aggregate load, information about expected load mixes is required. It was decided that example load mixes, representing bulk supply point load consisting of domestic load with additional industrial sector load, should be estimated for that purpose. In this way, all the load types considered in this thesis may be applied to form the corresponding aggregate

models. Where available, statistics on present and expected future contributions of individual load type/sub-type to overall aggregate load have been used. However, where statistics have not been available, estimations have been made. It is further assumed that in the future there will be no further changes in relevant legislative documents e.g. than no new harmonic standards will be introduced.

Statistics published by BERR (Department for business enterprise and regulatory reform), [81], giving the electric power consumption of household appliances in the UK in 2008, are used as the starting point for developing the example load mixes. Figure 6.8 shows these statistics.

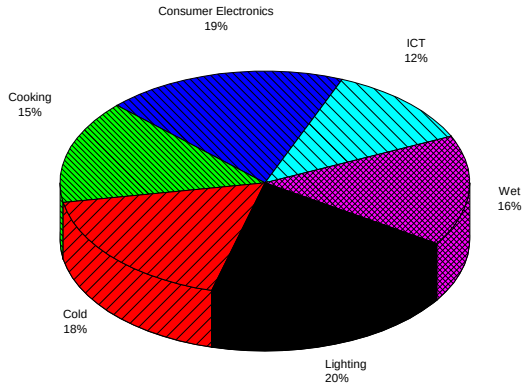


Figure 6.8: *Energy consumption by household domestic appliance category in 2008, [81].*

As can be seen from Figure 6.8, the presented statistics do not include resistive heating. From [114], it is estimated that of all UK households only 9% will have electric space and/or electric water heating. Therefore, in the developed load mixes electric heating is not considered as part of the domestic load mix, although, if required, this load type may be easily applied as an additional constant resistance load type.

In order to use statistics on categories of load in Figure 6.8 for this work, they should be matched with types and sub-types of loads developed in previous chapters. Additionally, the percentage contributions of each type and sub-type of load to each category should be found, by either using available statistics, or by estimating it where no statical data are available. The expected future changes in percentage contributions of each type/sub-type of load and overall contribution of considered category to the load mix was also investigated. If daily/weekly/seasonal load variations are of interest, then corresponding representative aggregate load mixes should be identified, and presented analysis should be repeated. Additionally, the purpose of the research presented in this thesis was not to identify daily/weekly/seasonal variations in aggregate loads, but to show how general analysis would

be done with the correct aggregate load mixes. Each load category defined in Figure 6.8 is now considered.

6.3.1 Consumer electronics and ICT load categories

The consumer electronics category consists of televisions, set-top boxes, external power supplies, etc., while the ICT load category consists of desktop PCs, laptop PCs, monitors, etc. From the work presented in Chapter 4, it was established that these electronic loads may be sub-divided into three distinct sub-types: SMPS without PFC, SMPS with passive PFC and SMPS with active PFC. The main source of statistical data used to define the contributions of each of these sub-types to the overall load was the Market Transformation Programme's (MTP) "WhatiF tool", [14]. Accordingly, unless otherwise stated, in the following sections presented statistics are derived using this tool.

6.3.1.1 ICT load

Currently, it is estimated that the majority of ICT load, around 63%, is made up of PCs. Of this load, 75% are desktop PCs and 25% are laptops. Computer monitors are estimated to use the second largest amount of power in the ICT category, accounting for some 26% of ICT load. This leaves the remaining 11% of ICT load made up of (e.g. cable modems, domestic routers etc.)

The ICT class of load is now sub-divided into expected SMPS sub-types. It is commonly known that modern desktop PCs will all have rated active power greater than 75W, and will therefore contain SMPS with either passive or active PFC. No specific statistics were available on the proportion of desktop PCs with active or passive PFC. From private discussions ([84]) and also considering that passive PFC is at present significantly cheaper than active PFC, it is assumed that currently the vast majority of SMPS found in desktop PCs (around 90%), will use passive PFC. This assumption is also further strengthened by the measurements of over 40 desktop PCs, performed during the course of the research, where it was found that only one desktop PC out of all measured had active PFC.

The majority of power supplies for laptop PCs are expected to have rated active power below 75W. However, there was no available statistics to specifically support this. The assumption is therefore made that 80% of laptop power supplies will have no form of PFC, and that 20% of laptops power supplies will use active power factor correction. The selection of active PFC in laptop over passive PFC is because of the physical size and weight of the passive PFC inductors, which would make this method of PFC unsuitable for portable laptop power supplies.

From [14], it is estimated that a typical LCD monitor consumes about 35W, while a typical CRT

monitor consumes about 50W. Accordingly, both of these loads will have SMPS with no PFC, as they will have rated powers below 75W. Finally, the remaining 11% of ICT loads, (routers, DSL modems, etc.) will as well be of active rated power less that 75W, and therefore contain SMPS with no PFC.

From the above discussion and statistics, the present day ICT load may be re-categorised by corresponding SMPS sub-type as follows: SMPS with no PFC 45%, SMPS with passive PFC 44% and SMPS with active PFC 11%.

6.3.1.2 General/consumer power electronic load

Currently in the UK, televisions are estimated to make up around 72% of the power consumed in the domestic power electronics sector. These televisions are predominately either cathode ray tube (CRT), liquid crystal display (LCD) or plasma televisions. It is also common for households to have one larger television, referred to as a primary TV, and one or more smaller televisions, referred to as a secondary TVs. Primary TVs account for around 72% of the total power demand due to televisions, and will usually have rated active powers greater than 75W, while secondary TVs account for the remaining 28% and usually have rated active powers less than 75W. As before, there is no data available that gives the explicit information on the type of PFC used in the power supplies of televisions with rated power greater than 75W. Therefore, it is again assumed that 90% of these television will employ passive PFC, with the other 10% using active PFC.

The remaining loads in the power electronics category, (e.g. secondary TVs, video players, set-top boxes and external power supplies) are all expected to have rated active power less than 75W, and will therefore require no form of PFC. Therefore, from the presented discussion and statistics, the power electronic load category may now be re-categorised into expected sub-type of SMPS load as follows: SMPS with no PFC 48%, SMPS with passive PFC 46% and SMPS with active PFC 6%.

6.3.1.3 Overall SMPS load

From the results previously presented in Figure 6.8, the ICT load category currently accounts for around 12% of total domestic power consumption, while the power electronics load category currently accounts for around 19% of domestic demand. These percentage contributions, along with the percentage contributions by sub-type of load for ICT and power electronic loads can be used to find the estimated present contribution of each sub-type of SMPS load to the total electronic load demand in the UK domestic sector, as shown in Table 6.1.

Table 6.1: *Present overall electronic load mix by SMPS sub-type.*

Type of SMPS	% contribution to electronic load
Active PFC	9
Passive PFC	45
No PFC	46

6.3.2 Future SMPS load mix

The predicted 2020 ICT and power electronic markets are now investigated, to obtain the corresponding expected SMPS sub-type load mix. Again, [14] is used as the main source for the presented analysis.

6.3.2.1 ICT load

By 2020, PCs will still account for the largest proportion of energy consumed in the domestic ICT class, some 64%. It is expected that laptops will make up 75% of the PC load, with desktop PCs accounting for the remaining 25%. The power consumption of individual laptops are expected to rise, as they will become replacements for desktop PCs. Therefore, it is likely that a higher proportion of laptop power supplies (than currently), will be of rated active power greater than 75W. Monitors are expected to account for 27% of domestic ICT load in 2020, when it is expected that there will be no CRT monitors. It is also predicted that the average monitor will draw around 55W, and that any envisaged energy savings due to replacing CRT monitors with more efficient LCD monitors will be offset by the increase in monitor screen size, [115]. Finally, the remaining 9% of ICT load will again have rated active power below 75W, and further breakdown of this load is not considered.

As there is once again a lack of available data regarding the exact breakdown on laptop rated powers, it is assumed that 50% of the future laptop load will be of rated power greater than 75W, and that they will have active PFC. Desktop PCs may have either passive or active PFC, but from private correspondence, [84], it is likely that in the future active PFC will be more prevalent than today. This is for two main reasons: firstly, the cost of active PFC is constantly decreasing, and secondly, active PFC allows for more efficient SMPS to be designed. The percentage of SMPS with active PFC is expected to be closer to 50%, compared to the current figure of 10%.

Again, the presented statistics and discussions may be used to re-categorise expected contribution of ICT load in 2020 by SMPS sub-type as follows: SMPS with no PFC 32%, SMPS with passive PFC 32% and SMPS with no PFC 36%.

6.3.2.2 Power electronic load

In 2020, televisions are expected to account for about 57% of the total energy consumption in the domestic power electronic load sector. CRT and plasma televisions are expected to be obsolete by 2020, with LCD television also reducing in number compared to current levels. It is expected that two new types of TVs will be common in the future, organic LED (OLED) televisions and field emission display (FED) televisions. Around 80% of the total power drawn by TVs in the predicted future load will be from TVs of rated active power of greater than 75W, i.e. primary televisions. The assumption is again made that of the televisions that require PFC, half will have active PFC, and half will have passive PFC. The remaining TV load made of TVs with rated active power under 75W and the other loads in this class, (set-top boxes, video players and external powers supplies) can be assumed to contain SMPS with no PFC. Again, from these discussions, the 2020 the power electronic load category in the UK domestic sector can be broken down as follows: SMPS with no PFC 23%, SMPS with passive PFC 23% and SMPS with active PFC 54%.

6.3.2.3 Overall SMPS load

By 2020, it is expected that the overall power consumption of the ICT load category will increase by 15%, with the power electronic category expecting to show a 40% increase. Taking these expected increases into account and combining them with the statistics presented in this section leads to the expected 2020 overall SMPS sub-type load mix as given in Table 6.2. It can be seen that there is expected to be considerable increase in the number of SMPS with no PFC in the SMPS load mix, due to the expected increased numbers of laptop PCs and set-top boxes. The implications of this change are discusses further throughout this chapter.

Table 6.2: *Predicted 2020 overall electronic load mix by SMPS sub-type.*

Type of SMPS	% contribution to electronic load	change in contribution since present
Active PFC	27	increased by three times
Passive PFC	27	approximately halved
No PFC	46	no changed

6.3.3 Cold and wet load categories

This load category includes refrigerators, freezers, room air-conditioners, washing machines, dishwashers etc. From Chapter 3, these types of loads are likely to be either single-phase directly connected or single-phase drive-controlled induction motors.

6.3.3.1 Cold loads

From Section 3.1.1, cold appliances will all be of constant torque mechanical load type. It is also expected that the type of SPIM used in these applications will be the RSIR motor, as refrigeration compressors do not require high running torques. There were no statistics available that detail how much of the present cold appliances loads may be drive-controlled motors. As application of this technology to these appliances is relatively new, it is therefore estimated that in the present load mix there are no drive-controlled motors in the cold load category.

The present total power consumption of the cold appliance load is estimated as 15479 GWh/yr, and is expected to be essentially the same in 2020, at 15780 GWh/yr [14]. This is because although there is expected to be an increased number of these appliances in the future (due to increased numbers of households), the increase in energy consumption will be offset by expected improvements in device efficiency, [115]. There were again no specific statistics available with regards to the estimated contribution of single-phase drive-controlled motors to this load category. It is was, therefore, estimated that 20% of cold domestic load will consist of lower-power SASD load in 2020, with the remaining 80% still consisting of directly connected RSIR single-phase motors.

6.3.3.2 Wet load

The present total power consumption of the wet appliance load is estimated at 14017 GWh/yr, which is similar to that of the cold appliance load. This total power consumption is made up from dishwashers (20%), tumble-dryers (29%), washer-dryers (18%) and washing machines (33%), where again data are taken from [14]. It is likely, due to relatively high running torque requirements, that tumble-dryers, washer-dryers and washing-machines will use RSCR single-phase induction motors. Dishwashers are expected to use RSIR single-phase motors. The above applications are all considered as quadratic torque mechanical load type. Again, there was no information with regards to present contribution of drive-controlled motors to this load mix and, accordingly, it is assumed that there are none at present.

In future, similarly and for the same reasons as discussed for cold load, the total power demand of wet load is expected to stay relatively constant, with a predicted value of 14930 GWh/yr. As there is once again a lack of data available for the expected contribution of drive-controlled motor load in the future, it is assumed that 20% of the wet loads will be made up of lower-power SASD load, with the remaining load consisting of 60% directly connected RSCR single-phase motors and 20% directly connected RSIR single-phase motors.

6.3.3.3 Overall cold and wet load

A type of load that has not been considered so far in the discussion of single-phase motor load is air-conditioning load. This is because this type of load is not significant in the UK domestic load sector. However, in the commercial load sector there is a certain proportion of air-conditioning load and elsewhere in Europe this type of load can make up a large proportion of demand in the domestic sector. Therefore, it is important to represent this load type in the presented analysis. Accordingly, this load type is assumed to contribute 20% to the total power demand in the single-phase motor load category, (i.e. both wet and cold loads). For the purpose of this analysis, the percentage contribution of this load type is assumed to remain the same in 2020.

From the presented statistics, estimations and discussions for the cold and wet load categories, the contributions of SPIMs and SASDs to the present and future domestic demand may be estimated. This is summarised in Table 6.3. It should be noted that the estimated percentage contributions presented in Table 6.3 are not supported with any statistical data, simply because there is not any available.

Table 6.3: *Single-phase directly connected and drive-controlled motor loads.*

Load type	Contribution to present load (%)	Contribution to future load (%)
RSIR	50	35
RSCR	30	25
Lower-power SASD	0	20
Higher-power SASD	20	20

6.3.4 Lighting load category

Presently, lighting in the UK domestic sector consists of incandescent lighting, halogen lighting and fluorescent lighting. Incandescent and halogen lighting can be classed as resistive load, and currently make up around 91% of the total energy demand in this sector. Fluorescent lighting make up the remaining 9% of lighting load. As discussed in Chapter 5, there are moves towards a wholesale substitution of incandescent lighting with more efficient fluorescent lighting. Thus, it is assumed that in 2020 all domestic lighting load will be made up from CFL lighting. If all incandescent light sources are replaced by CFL lighting, [14] predicts that the 2020 energy demand due to lighting will be approximately a third of the present value. This is because although CFL lighting is about five to six times more efficient than incandescent lighting it tends to be left on for longer and additionally there will also be increased numbers of households by 2020.

6.3.5 Cooking load category

This load category is not considered in any detail, as it is assumed to be purely resistive for the purposes of this analysis. However, a proportion of this load will be made up of microwave ovens which are non-linear loads and are expected to have similar characteristics to other non-linear loads considered in this thesis. Statistics from [14] predict that there is not likely to be any significant change in energy demand in this sector by 2020.

6.3.6 Overall expected load mixes

As discussed previously, an industrial load is also to be added to the domestic load mix. The present industrial load mix is taken as being made up of 80% directly connected lower-power three-phase motors, with half of these motors mechanically loaded with constant torque and the other half with quadratic torque mechanical torque load. The remaining 20% of the industrial load consists of 10% V/Hz closed-loop controlled ASDs operated in continuous mode, and 10% of V/Hz closed-loop controlled ASDs operated in discontinuous mode. The total power demand of the industrial load is selected to represent 20% of the present load mix. The predicted future industrial load mix uses the same types of motors and drives, but this time the percentage of drive-controlled motors in the industrial load mix is increased to 50%, to represent more intensive use of this load type.

From the statistics and estimations in this section, present and future example load mixes may be produced. These load mixes are expressed by load type and sub-type, as defined in this thesis. Figure 6.9 shows the present load mix, while Figure 6.10 show the predicted future (2020) load mix. It should be noted that the subject of this thesis was not accurate identification of present and future load mixes, although, significant efforts were made to review available statistics and provide realistic estimations. The aggregate load mixes used in this thesis, should be additionally validated by, e.g. measurements at corresponding system buses.

6.4 Active and non-active power characteristics of aggregate present and future load mixes

The present and future load mixes developed in the previous section are now used to construct aggregate loads. These aggregate loads are formed from proposed exponential, polynomial and generic analytical models of each load type/sub-type presented in this thesis. To provide comparison, the same aggregate loads are also formed using previously developed exponential models of individual load types, as presented previously in Table 1.1.

The relevant aggregation methods described in Section 6.2 are used to form each aggregate load. In order to investigate the effects of system voltage distortion on aggregate load

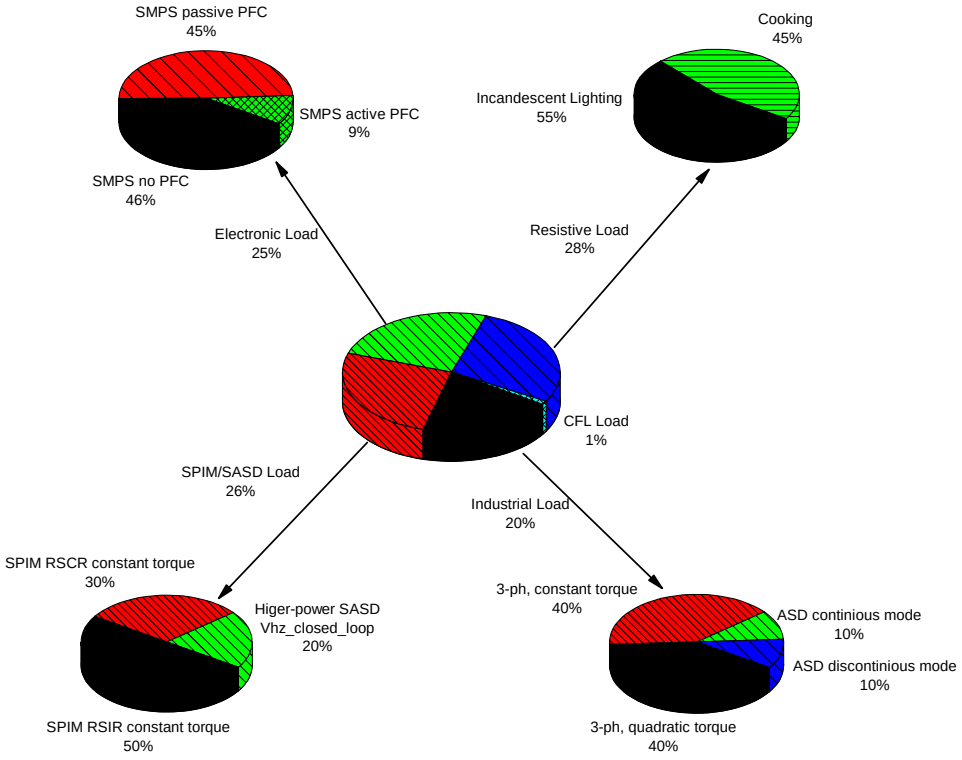


Figure 6.9: *Estimated present load mix.*

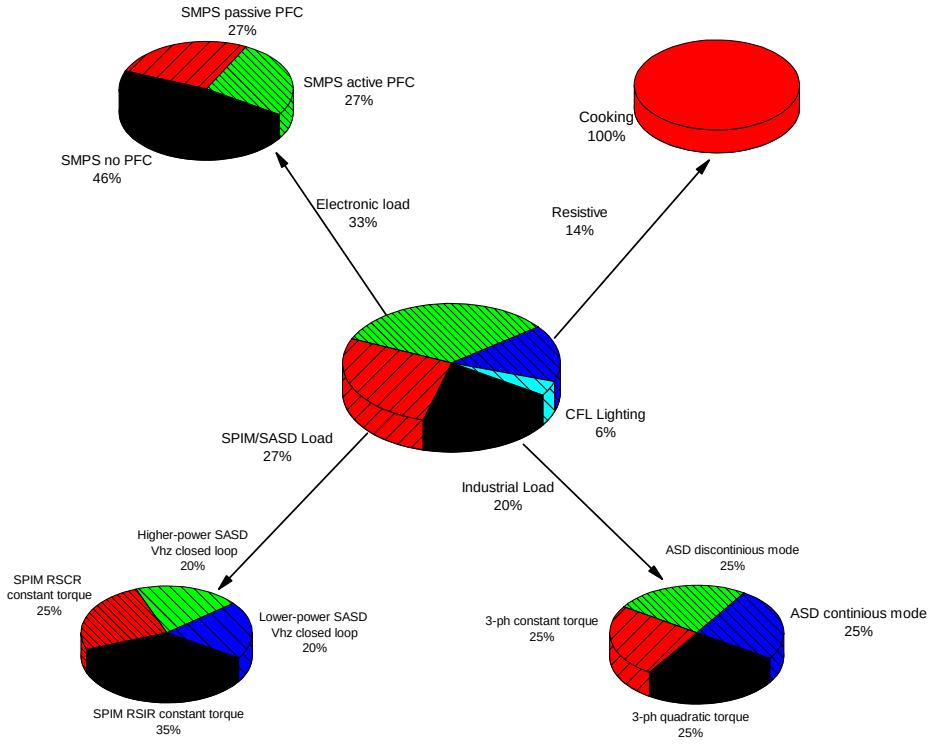


Figure 6.10: *Estimated future (2020) load mix.*

characteristics, generic analytical models were aggregated for applied "typically distorted" and "heavily distorted" system voltages, (Section 2.12.2), as well as for ideally sinusoidal supply voltage. In all cases, the value of system impedance was taken as the nominal value used in this thesis (Section 1.8).

Table 6.4 shows the polynomial and exponential interpretations of present and future aggregate load formed from generic analytical models with applied sinusoidal system voltage. The polynomial and exponential interpretations of individual type/sub-type load were also aggregated using expressions (6.1) to (6.5) to form aggregate load models. It was found that these load models very closely matched the polynomial and exponential interpretations of present and future aggregate load formed from generic analytical models with applied sinusoidal system voltage. This is because the proposed polynomial and exponential models of the individual type/sub-type load are direct interpretations of corresponding generic analytical models, of relevant type/sub-type loads, with applied sinusoidal voltage and nominal system impedance. Therefore, the aggregate loads formed from individual analytical models (with applied sinusoidal voltage and nominal system impedance) and individual polynomial/exponential models will have the same P-V, Q_1-V and PF_1-V power demand characteristics, although latter models will not contain any further information about the aggregate load. Accordingly, only polynomial and exponential coefficients of the aggregate load formed from analytical models are shown in Table 6.4. The polynomial and exponential model coefficients of the present and future aggregate loads formed using previously proposed (existing) individual models of each load type are also shown in Table 6.4.

Table 6.4: *Exponential and polynomial model coefficients of present and future load mixes.*

PF_1	Exp. Model		Polynomial Model					
	np	nq	Z_p	I_p	P_p	Z_q	I_q	P_q
Present aggregate load from proposed models								
0.934	0.59	1.27	0.48	-0.38	0.89	0.54	-0.61	0.45
Present aggregate load from existing models								
0.9	1.32	3.31	0.52	0.27	0.21	5.01	-6.77	2.76
Future aggregate load from proposed models								
0.97	0.31	1.42	0.43	-0.56	1.13	0.39	-0.42	0.29
Future aggregate load from existing models								
0.86	1.33	3.4	0.46	0.38	0.16	6.25	-8.84	3.59

The characteristics of the aggregate load models of present and future load mixes are plotted in Figures 6.11 and 6.12. As before, the polynomial and exponential models have almost identical P-V, Q_1-V and PF_1-V power demand characteristics and are therefore shown as one plot in the figures. The standard constant power, current and impedance load models (Section 1.1) are also shown in Figures 6.11 and 6.12.

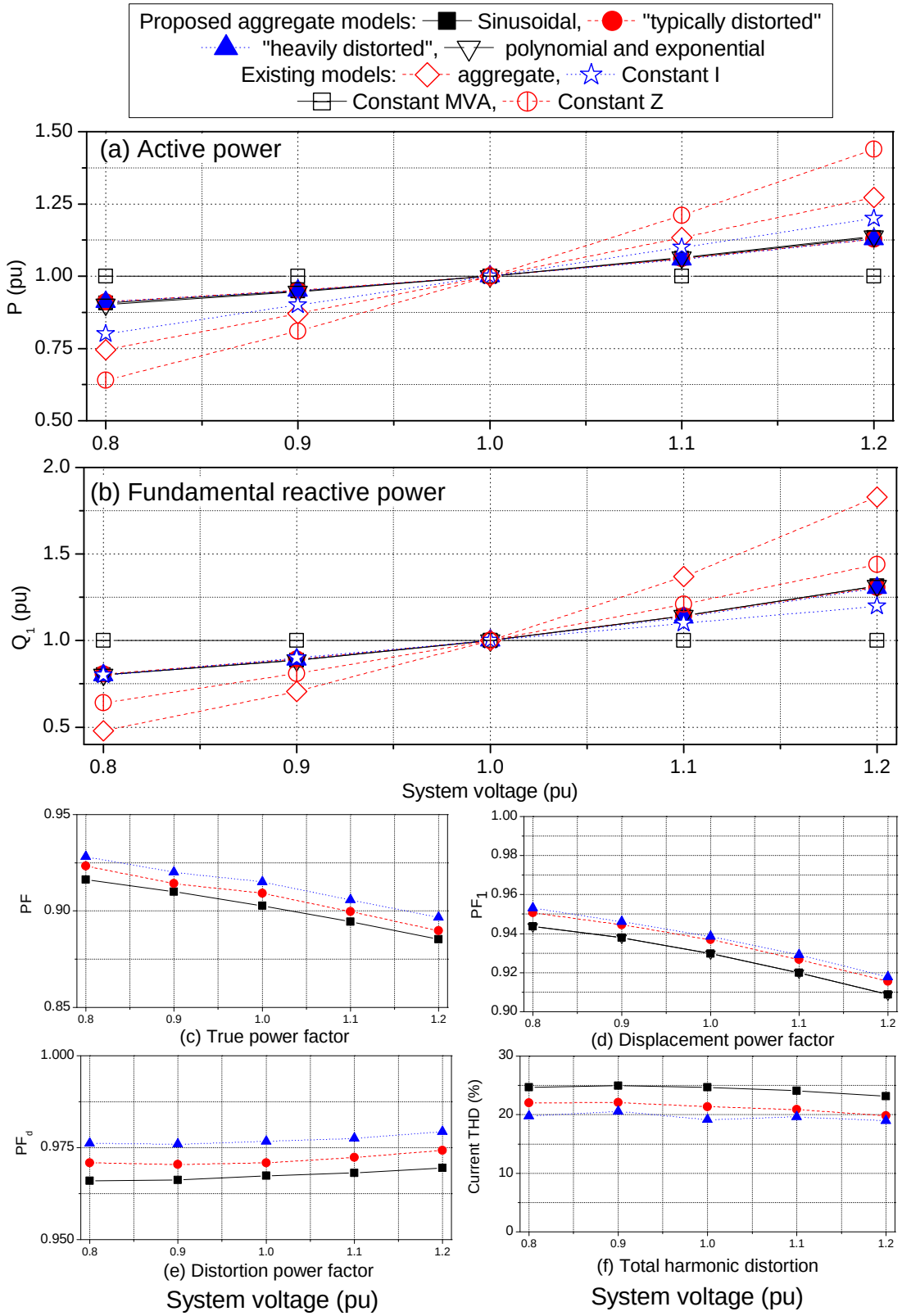


Figure 6.11: *Comparison of results from proposed and existing load models for present load mix.*

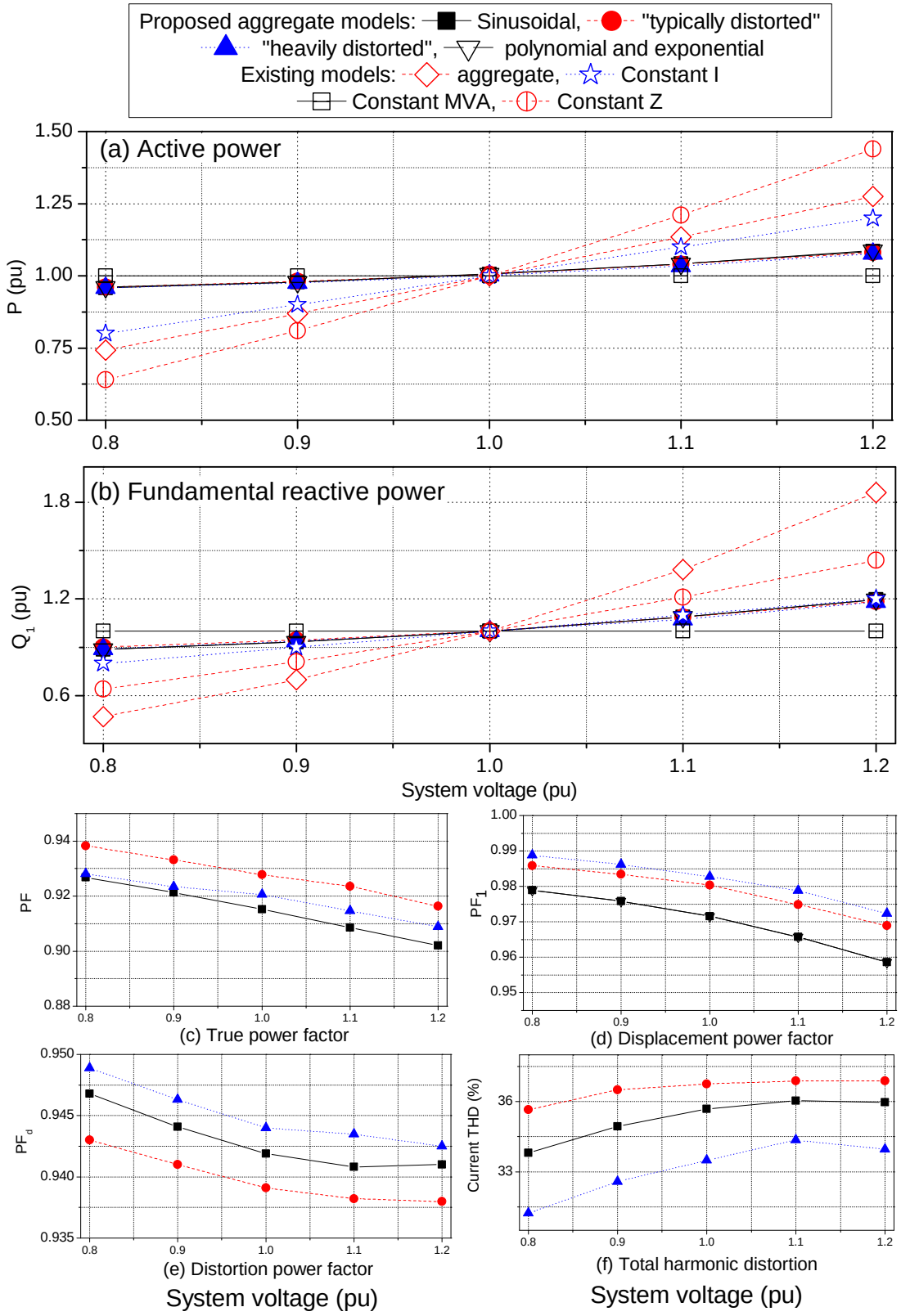


Figure 6.12: *Comparison of results from proposed and existing load models for future (2020) load mix.*

It can be seen from Table 6.4 and Figures 6.11 that the proposed load models predict that the present aggregate load will have a closer to constant active power characteristic than what is predicted by the aggregate load formed from existing load models, (i.e. np = 0.59 for proposed model compared to 1.32 for existing model). This difference can mainly be attributed to the representation of power electronic loads in previous load models, i.e. they are represented as having constant impedance (np = 2) P-V characteristics, compared to constant power (np = 0) P-V characteristics in the proposed models. There is also a disagreement in Q_1-V characteristics between proposed and existing aggregate loads for the present load mix. Again, a major reason for this disagreement is the difference in the representation of Q_1-V characteristics of electronic loads between proposed and existing models. Existing models of electronic loads represent them as inductive and operating with $PF_1 = 0.8$, while proposed load models represent electronic loads as either capacitive loads $PF_1 \approx 0.99$, inductive with $PF_1 \approx 0.97$, or resistive loads with PF = 1 (presence/absence of PFC).

Differences between proposed and existing models of single-phase and three-phase directly connected motors, as well as the addition of drive-controlled motors in the proposed aggregate load, will also influence the difference between P-V, Q_1-V and PF_1-V characteristics of the present aggregate load formed from proposed and existing load models. The models of fluorescent lighting in the two aggregate loads will have very similar P-V characteristics. However, the model of existing fluorescent lighting represents LFLs with magnetic ballast, which are inductive loads ($PF_1 = 0.9$, 'lagging') while the the proposed fluorescent lighting model represents CFLs, which are capacitive loads ($PF_1 = 0.9$, 'leading').

In the future, the proposed aggregate model predicts that corresponding P-V characteristics will become even more close to constant power characteristics (than presently), np from 0.59 to 0.31. It also predicts that load displacement power factor will improve considerably, and that Q_1-V power demand characteristics will move closer to constant impedance than previously (nq from 1.27 to 1.42). These significant changes are due to the increased amount of non-linear loads expected in the future and associated decrease in linear loads (replaced with non-linear loads).

In the future, electronic load (which has constant P-V characteristics) is expected to represent a greater proportion in the total (considered) aggregate load mix than presently. Furthermore, in the future load mix, incandescent lights (constant impedance P-V characteristics) will be replaced by CFL lighting (constant current P-V characteristics), which will 'push' aggregate load characteristics further away from constant impedance. Therefore, the electronic and CFL load types will be mainly responsible for reduction in the np coefficient of the considered future load mix, i.e. making this aggregate load closer to constant power P-V characteristics.

The addition of drive-controlled single-phase motors and increased numbers of drive-controlled

three-phase motors will increase displacement power factor of the future aggregate load, as these loads will replace directly connected single-phase and three-phase motors, which operate at significantly lower displacement power factors. Additionally, and as discussed, CFL load is capacitive, operating at a relatively low displacement power factor, which will provide some compensation for reactive power demand of other, inductive loads, further improving the displacement power factor of the proposed future aggregate load (electronic and SASD loads with no PFC are also capacitive but they operate at high values of PF_1, in sinusoidal situations, and will therefore supply little reactive power).

The aggregate load model formed from existing models predicts little difference in P-V and Q_1-V power demand characteristics between present and future load mixes. It also predicts that displacement power factor will reduce, contrary to results with proposed load models. This reduction is almost entirely due to the existing model of electronic loads, in which the displacement power factor of these loads is 0.8 (”lagging”).

It can be seen from Figures 6.11 and 6.12 that distortion in the system voltage will have no significant effect on the P-V and Q_1-V power demand characteristics of both present and future aggregate load mixes (for aggregate load formed from generic analytical models). Therefore, both the polynomial and exponential interpretations are able to accurately predict these characteristics.

Distortion of the system voltage, however, will affect the displacement power factor of both considered load mixes, showing an increase in displacement power factor with increased voltage distortion. For present load mix, displacement power factor increases from 0.929 for sinusoidal conditions, to 0.939 for heavily distorted conditions. For future aggregate load, displacement power factor increases from 0.97 to 0.983. This increase in PF_1 is attributed to lower-power SASD, SMPS with no PFC and CFL loads, which will all show reduction in PF_1 on system voltage distortion. As these load are capacitive, a reduction in their PF_1 leads to an increased value of PF_1 in the aggregate load, as it will compensate inductive load. Other considered types of non-linear loads show very little variation of PF_1 with system voltage distortion. Accordingly, as PF_1 is used to calculated nominal Q_1 (i.e. $Q_{1,nominal} = P_{nominal} \cdot \tan(\cos^{-1}(PF_1))$), distortion of the system voltage will decrease fundamental reactive power demand (although, as discussed above it will not alter the ‘shape’ of the Q_1-V characteristic). For the present load mix, the difference in PF_1 between sinusoidal and “heavily distorted” system voltage represents a difference in nominal Q_1 demand of about 8%, while in the future load mix it represents a difference of about 25%. Polynomial and exponential models cannot consider the effects of system voltage distortion, as they assume all system bus voltages to be ideally sinusoidal. Standard load flow analysis also assumes sinusoidal system voltage, and does not consider the alteration in fundamental reactive power flow with system voltage distortion. The following section investigates the effects of presented aggregate load on

a typical UK/Scotland distribution network.

Finally, the results for THD and PF_d characteristics in Figures 6.11 and 6.12 are directly related to the associated harmonics of the aggregate loads, and are discussed in more details in Section 6.6.

6.5 Standard load flow studies

The analysis in the previous section compared the P-V, Q_1-V and PF_1-V characteristics of aggregate loads formed from proposed and existing load models. The analysis included both present and future domestic and industrial sector load mixes. This section investigates effects of considered different load models on a typical UK distribution network.

6.5.1 Selected network

The distribution network selected, for the comparative analysis of different aggregate loads was taken from the United Kingdom Generic Distribution Systems (UKGDS) research project. UKGDS is a recent collaboration between the DTI (now BERR), Imperial College London, the University of Manchester and the University of Strathclyde. This project has developed typical generic models of the distribution systems in the UK, with the goal of providing a common research source for simulations and analysis. The project developed several example networks, with network component parameters obtained from the review of UK electrical utilities' long term statements. Further details of these network models can be found in [116].

One section/part of a larger radial UKGDS network ("EHV Network 2", [116]) was selected for the analysis in this section, Figure 6.13. The network was implemented in PSS/E software, [117]. In the selected UKGDS network model, all loads are represented as constant MVA loads with displacement power factors of 0.95 lagging. Although no documentation could be found that provides reasons for this selected load model, constant MVA load is often assumed to represent a 'worst case' load model, which may be the reason why this load model is selected in UKGDS.

6.5.2 Performed analysis

A standard method of comparing the effects of different loads models on a power system network is to perform investigations of the system's load meeting capacity (LMC) with considered different load models. The value of system LMC is found by increasing the power of each load on the network simultaneously as a percentage of their base case values. As the power demand at each load bus is increased, the bus voltage will reduce, and when bus

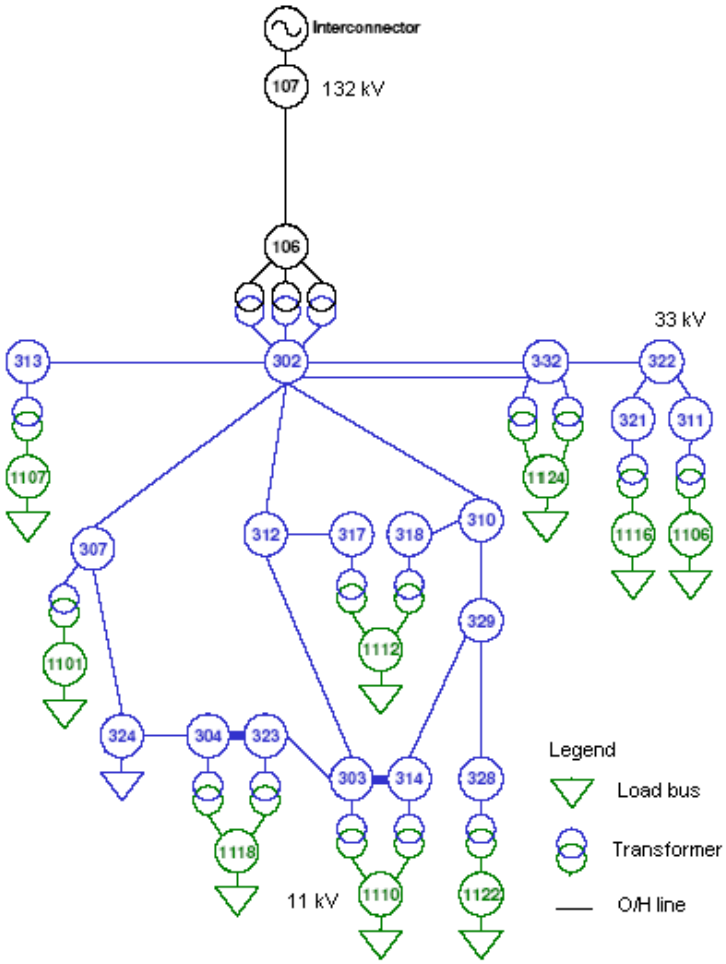


Figure 6.13: *Example of a typical UK distribution network.*

voltage is less than 0.8pu, this is considered as an unacceptable operating condition and the corresponding load is taken as the system LMC value.

The proposed generic analytical models can not be directly implemented in PSS/E. Therefore, polynomial interpretations of the aggregate of these individual load models, for both present and future load mixes (as given Table 6.4), were applied to the PSSE network model instead. As has been discussed in the previous section distortion in the system voltage will cause the displacement power factor of the aggregate analytical load to reduce. There is no mechanism to model non-sinusoidal supply conditions in PSS/E so the effect of system voltage distortion on aggregate load characteristics is simply modelled by performing LMC analysis at two values of PF_1, one value for applied sinusoidal conditions and one value for "heavily distorted" supply conditions. This method is basic, however, it does give an insight into the likely effects of voltage distortion on the considered system. The aggregate load developed from existing individual load models was also applied to the PSS/E network model, (as given

Table 6.4). Finally, three general load models (constant power, current and impedance) were also considered, with PF_1 of these loads taken to be 0.95. The characteristics of each aggregate load model were applied to every load bus, and LMC analysis was performed.

The results of this analysis (Figure 6.14) are shown for load bus 1122 from Figure 6.13. This bus was selected as it represent the end of a long radial feeder, where voltage problems are most likely to occur. It should be noted that for the analysis presented in this thesis it is not important which specific network bus is monitored. This is because this thesis presents a general comparative analysis of the effects of different loads models on network performance and all network load buses will exhibit the same general effects to a greater or lesser extent (depending on actual bus loading conditions and network impedance at the bus of interest).

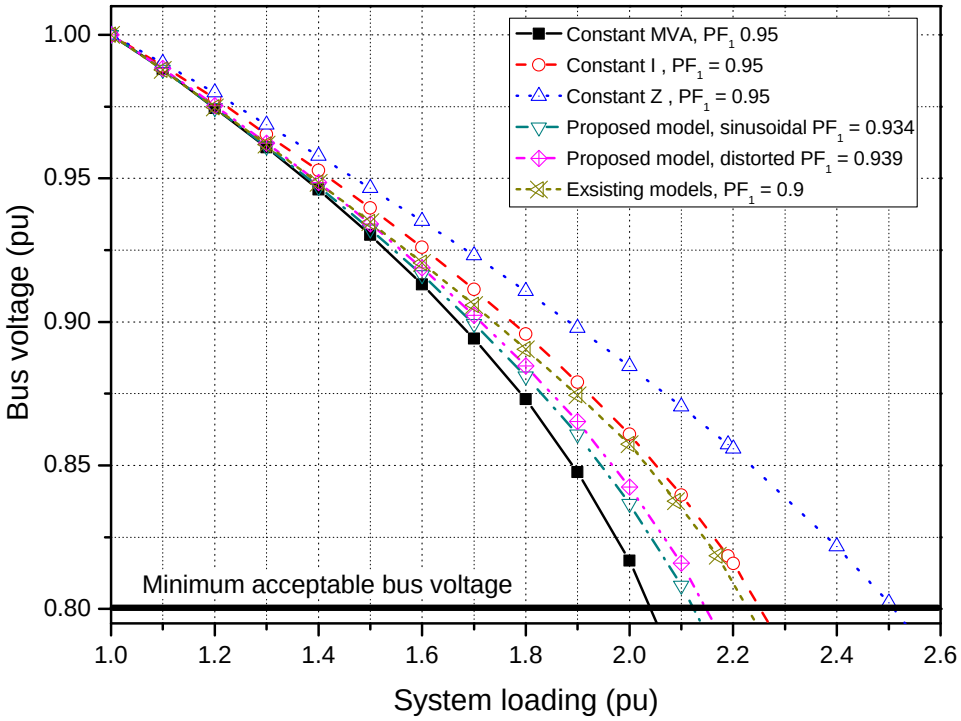
6.5.3 Discussion of results

The results of the analysis in Figure 6.14(a) show that the load meeting capacity (LMC) of the considered system is least when the load was assumed to be constant MVA, and greatest for constant impedance load, for both present and future load mixes. It can be seen that the proposed load model, for sinusoidal supply conditions, predicts that the system LMC will be less than the value predicted by existing aggregate load models. Further, these results also show that distortion of the system voltage will also have an effect on the system LMC.

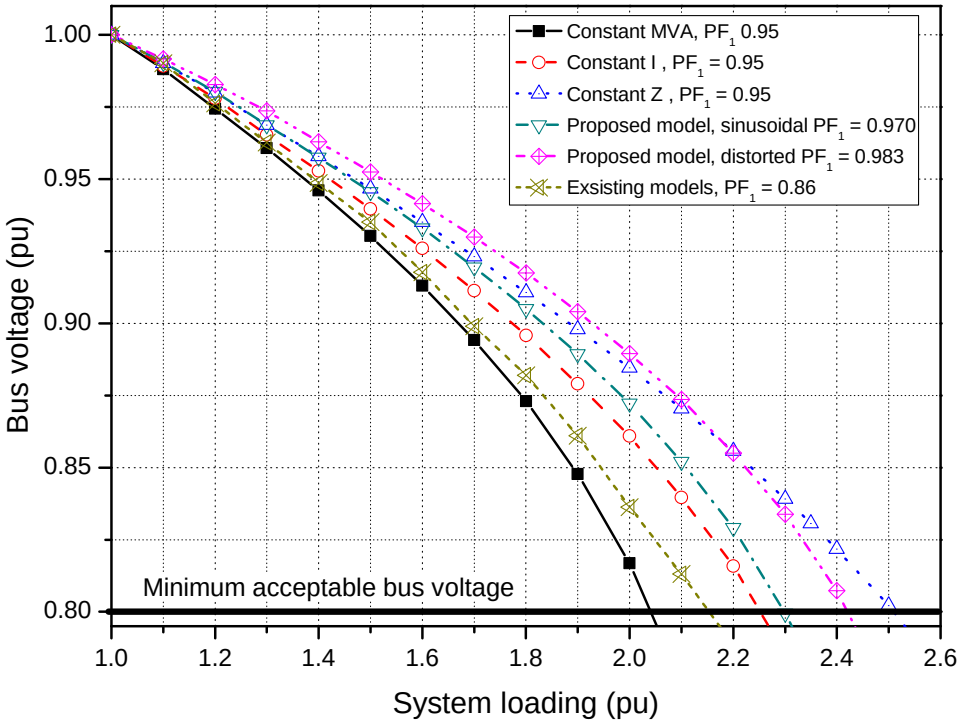
From the results presented in Figure 6.14(b), it can be seen that the proposed aggregate load model predicts that system LMC will increase in the future, while existing load models predict that system LMC will reduce in the future. It can further be seen that the proposed aggregate load for distorted voltage supply conditions predicts a higher system LMC than aggregate load for sinusoidal supply conditions. This is due to the improved displacement power factor of the aggregate load for distorted supply conditions, compared with aggregate load for sinusoidal conditions (improved PF_1 influences that load draws less fundamental reactive power).

The results of the presented analysis show relatively large differences in network responses to different load models. The proposed aggregate load models predict that the future system may accommodate higher power flows than presently, while existing aggregate load models suggest the opposite. The results also highlight the differences between the characteristics of present and future proposed aggregate loads. It can be seen that the future load will become less inductive which will improve system load meeting capacity.

Although the presented analysis is simple, it still highlights the importance of accurate load representation as this will have significant effect on the performance of the considered network. The presented results also suggest that assumptions about sinusoidal supply conditions in standard load flow analysis, when aggregate load has a high proportion of non-linear loads, may



(a) Present load mix



(b) Future load mix

Figure 6.14: *Comparison of the effects of different load models on system bus voltage and LMC, at load bus 1122.*

lead to error. This is an important conclusion that should be considered further, but it is outside the scope of this thesis, and therefore is recommended for further work (see Section 7.2).

6.6 Harmonic characteristics of present and future load

As the proposed generic analytical models of each type and sub-type of load are able to predict their actual current waveforms, they also provide information on their harmonic content. Therefore, these load models allow for analysis/assesment of aggregate load harmonic content.

References [118–121] have discussed that the harmonics of an aggregate load are often considered as random variables, characterised by probability densities and deterministic functions. These probability densities and deterministic functions are affected by the types of non-linear load in the considered aggregate load. It has been shown in this thesis that specific load types, due to harmonic legislation, should be broken into several sub-types. These load sub-types have significantly different harmonic characteristics. Although references [79], [122] and [123] have considered the harmonic characteristics of the electronic load type, this work has only considered electronic loads with no PFC, as this research was performed over ten years ago (when IEC:61000 3-2 harmonic limits, [30], were not mandatory in the EU). More recent research, for example [124] (2007) and [125] (2008), has also not considered the effects of harmonic legislation on the harmonic characteristics of typical aggregate system load. Additionally, none of the above mentioned research has considered the new non-linear loads types expected to increase in the future, namely CFL lighting and single-phase drive-controlled induction motors.

This section aims to show the versatility of the developed load models by using them to investigate expected harmonic interactions between different load types and sub-types. It should be noted that the aim of this thesis was not to perform detailed stochastic or deterministic analysis with developed load models, although the presented analysis is making this possible.

As well as investigating the effects of harmonic interactions between new types and sub-types of loads, comparative analysis is also performed between present and future load mixes. This analysis investigates the likely effects on aggregate load harmonic characteristics of the expected changes in numbers, type and sub-type of non-linear loads in the future. Furthermore, in order to complete the analysis and fully demonstrate the versatility of the developed load models, the developed models are applied to a simple two bus system, and the associated distortion of system bus voltage is investigated.

6.6.1 Harmonic cancellation

When different types and sub-types of non-linear loads are connected to a point of common coupling, i.e. to system bus, the aggregate harmonic content of these loads is not a simple sum of the harmonic magnitudes of each load. This is because the current drawn by each type and sub-type of load will contain harmonics with different phase angles. Therefore, as harmonics are vector quantities, aggregate harmonics magnitudes will not be obtained as an algebraic sum of individual load type/sub-type harmonics magnitudes. This effect is known as harmonic cancellation. Cancellation between specific harmonics of each load type/sub-type is greatest when harmonic phase-angles are 180° relative to each other, and smallest when the harmonics are in phase with each other.

To a certain extent, harmonic cancellation will also occur in same type/sub-type load, although this effect is much lower than cancellation between different types and sub-types of loads. Developed load models in this thesis can be used for this analysis, which is also expected to be the subject of the further work, (see Section 7.2).

An indicator used to quantify harmonic cancellation is known as the diversity factor, [79]. The diversity factor is the ratio between the vector sum and the algebraic sum of the individual load type/sub-type current harmonics in the considered aggregate load, (6.6). Diversity factor of one indicates no harmonic cancellation, while diversity factor value of less than one indicate harmonic cancellation in the aggregate load. The effects of harmonic cancellation on the present and expected future domestic sector load mixes are investigated in the following sections.

$$DF_h = \left| \frac{\sum_{i=1}^{N} I_h^i}{\sum_{i=1}^{N} \left| I_h^i \right|} \right| \tag{6.6}$$

Where: $I_h^i = \left| I_h^i \right| \angle \theta_h^i$ = harmonic current of order h injected by the i_{th} load, θ is harmonic angle and N is the number of loads.

6.6.1.1 Present aggregate load mix

The percentage contributions of each load type and sub-type corresponding to the "present load mix" were applied to the developed analytical aggregation code (see Section 6.2.2) to form this aggregate load. The system impedance was taken as the nominal (see Section 1.8). The individual load type, sub-type and aggregate current waveforms are shown in Figure 6.15. This figure illustrates how the aggregate current waveform is formed, further to the explanations in Section 6.2.2. The associated harmonic magnitudes and angles of corresponding load

types/sub-types and of the aggregate load are shown in Figures 6.16 and 6.17, respectively.

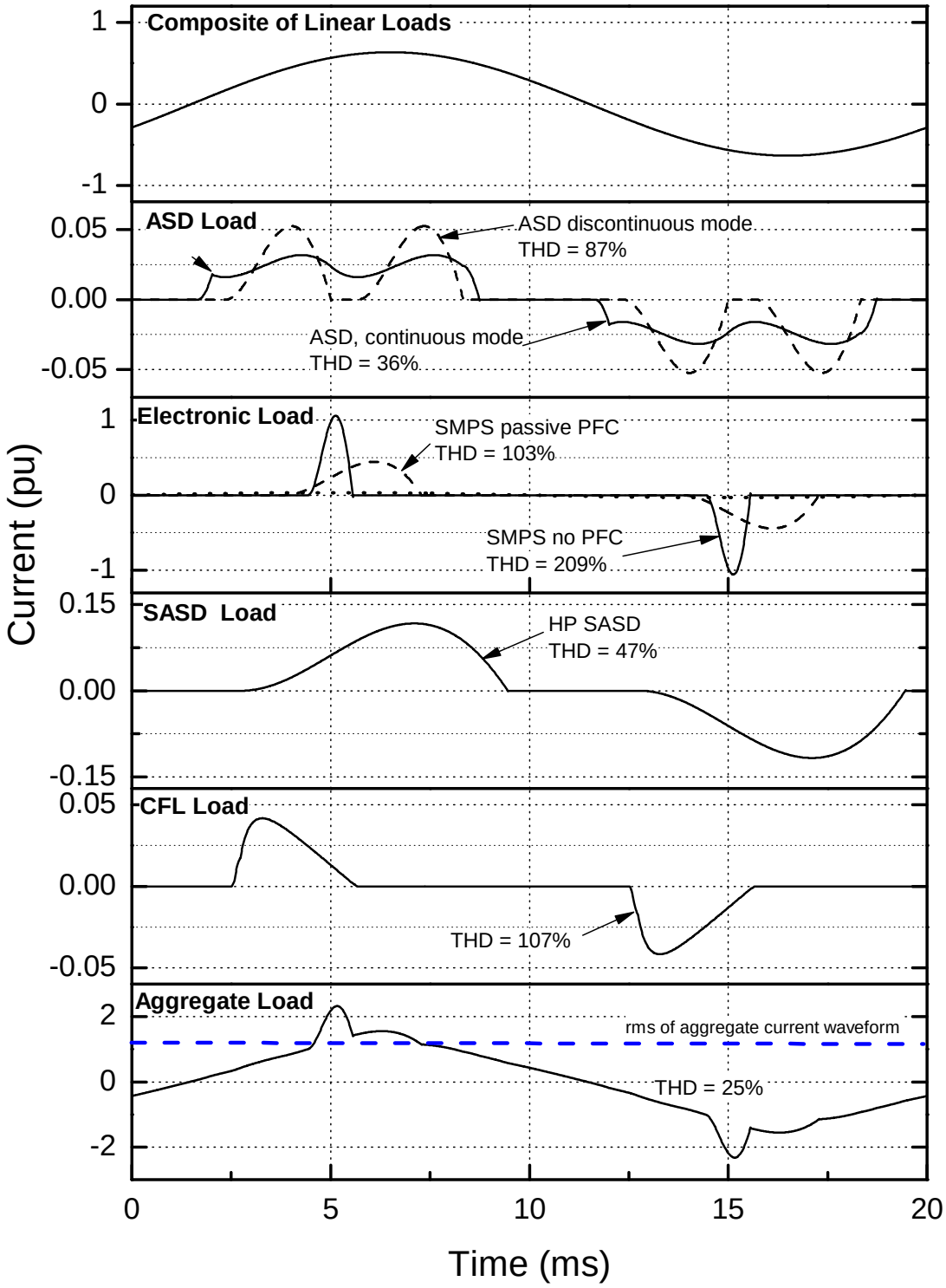


Figure 6.15: *Current waveform of present aggregate load and corresponding waveforms of individual load types/sub-types, normalised to a base of the rms value of aggregate load current.*

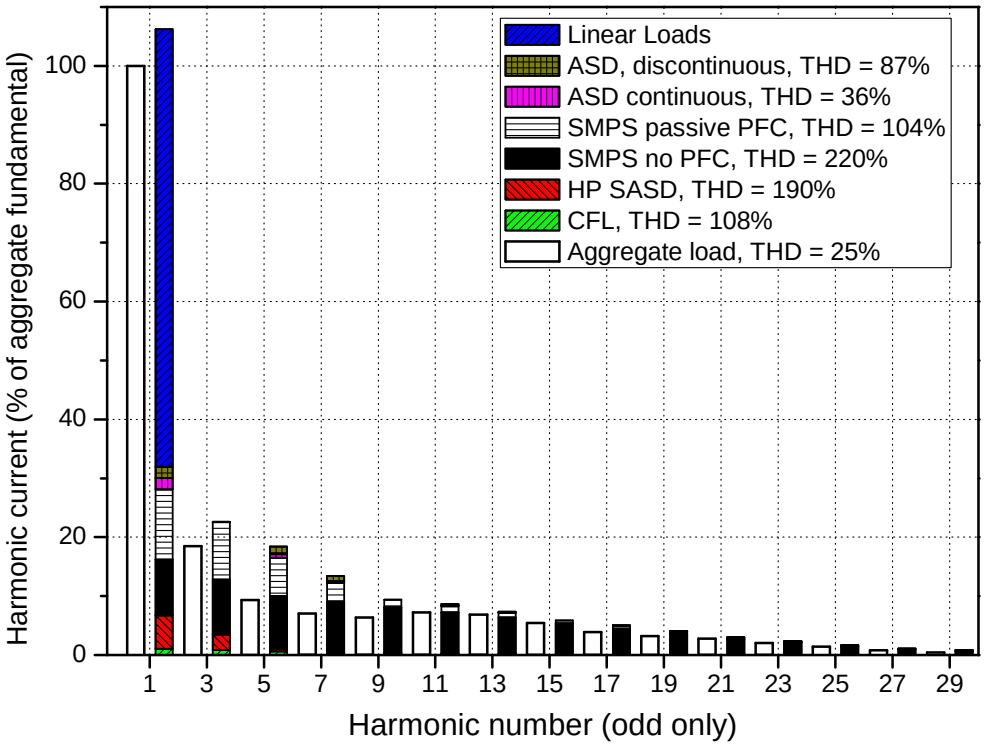


Figure 6.16: *Present load mix harmonic magnitudes.*

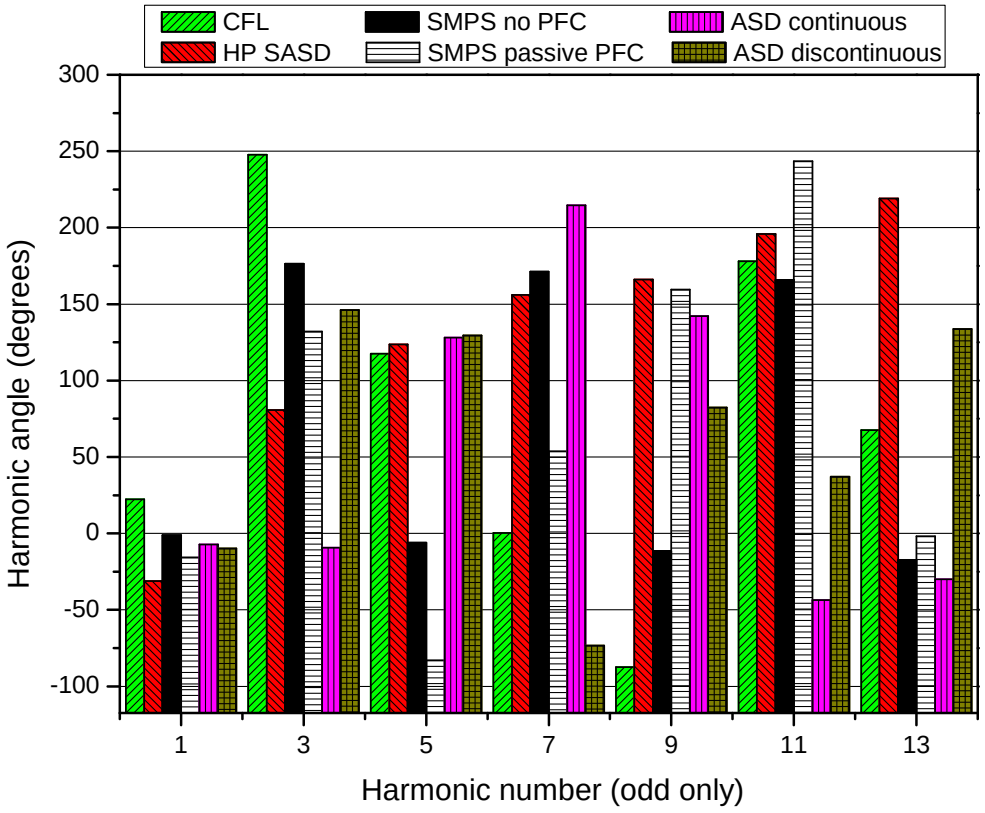


Figure 6.17: *Present load mix harmonic angles.*

The phenomenon of harmonic cancellation is clearly shown in Figure 6.16, where it can be observed that the harmonic content of the aggregate load is lower than the summation of the individual load harmonics. This figure also shows that the harmonic contribution of the CFL, SASD and ASD load types/sub-types are small compared to that of the electronic load type/sub-types. This is due to a low contribution to the total power of the considered load mix, Figure 6.9. The contribution of the CFL load type to the aggregate harmonic content is in fact so small, that it may effectively be neglected for all considered harmonics. The magnitude of the higher-power (HP) SASD' current harmonics beyond the 3^{rd} harmonic will also become negligible. Both ASD load sub-types have no 3^{rd} harmonic content and will only contribute a small amount to the aggregate load's 5^{th} and 7^{th} harmonics. The harmonic content of the SMPS with passive PFC decreases significantly as harmonic number is increased, and it is essentially zero beyond the 13^{th} harmonic. Thus, the SMPS with no PFC will dominate the harmonic content of the aggregate load beyond the 13^{th} harmonic, while also having very significant influence on the lower order harmonics.

There is only a small difference between the phase angles of the 3^{rd} harmonic of SMPS with passive PFC and SMPS with no PFC, and hence little cancellation is seen for this harmonic. Therefore, the majority of cancellation of this harmonic is attributed to CFL and higher-power SASD loads. However, for higher order harmonics, the difference in harmonic phase angle is greater between SMPS with passive PFC and SMPS with no PFC. Therefore, for harmonic orders greater than the 3^{rd}, and in particular the 5^{th} and 7^{th} harmonics, the presence of SMPS' with passive and no PFC in the load mix will not significantly increase the harmonic content of the aggregate load, due to harmonic cancellation between these two load sub-types.

This is an interesting result, as it shows clearly the importance of dividing load types into corresponding sub-types. In this case, two sub-types of the general electronic load type are cancelling each other's harmonics. Furthermore, these result also show that the SMPS with no PFC is dominating the harmonic content of the present load mix, while other non-linear loads have relatively little effect.

6.6.1.2 Future aggregate load mix

The expected future (2020) load mix is now used to form the aggregate load in the same way in which the present load mix was formed in the previous section. Figures 6.18 and 6.19 show associated harmonic magnitudes and angles of all considered load types, sub-types and aggregate current waveforms.

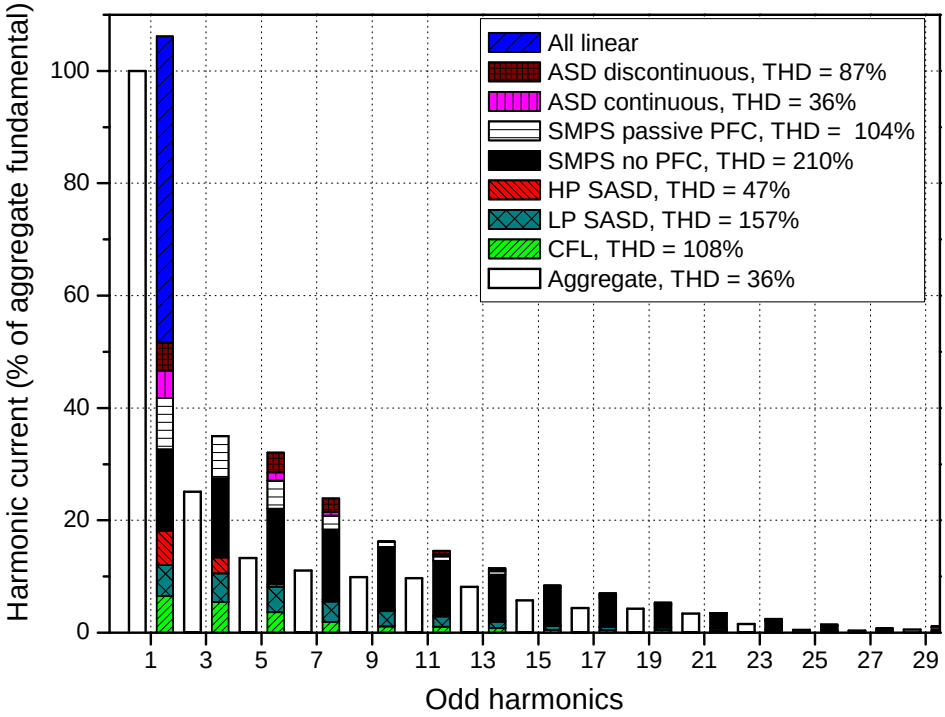


Figure 6.18: *Future load mix harmonic magnitudes.*

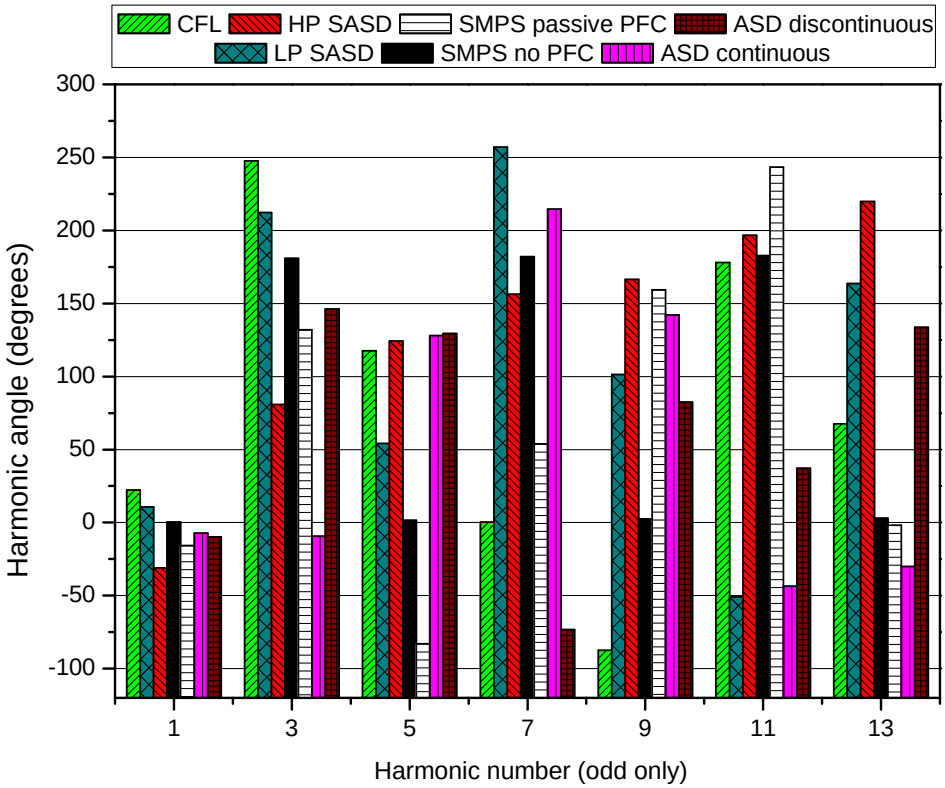


Figure 6.19: *Future load mix harmonic angles.*

It can be seen from the results presented in Figure 6.18 that in the future load mix the aggregate load current waveform is predicted to have a THD of 36%, compared to 25% of the present load. This is due to the increased contribution of non-linear loads to the total load mix and corresponding decrease of contributions of linear loads, (i.e. due to replacing of incandescent lighting with CFL lighting, and replacing of directly connected motors with drive-controlled motors). The results also show that there is once again a significant cancellation in the future load harmonics.

Figure 6.20 compares the 3^{rd} to 29^{th} harmonic magnitudes of the present and future aggregate load mixes, as well as associated diversity factors. The results show that the diversity factors of all considered future load harmonics are lower than those of the present day load mix load. This is because there is more diversity (i.e. higher numbers) of non-linear loads in the future. The expected contribution of the CFL increase from 1% of the total in the present load mix, to 6% in the future load mix; lower-powers SASD increases from 0% to 5.4%, for both types of ASDs from 2.5% to 5%, for SMPS with no PFC from 10% to 15%, and for SMPS with passive PFC it decreases from 12% to 9%. Accordingly, there is more harmonic cancellation between the non-linear loads, because, as can be seen from Figure 6.19, all of these loads will have different harmonic angles to each other. Again, it is seen that much of this cancellation will be due to SMPS' with no PFC and SMPS' with passive PFC. Although there is more harmonic cancellation in the aggregate future load mix, the harmonic content of this aggregate load is still significantly greater (50%) than that of the present day load mix. This is because of increased numbers of non-linear loads and decreased numbers of linear loads in the future load mix.

These results again show the importance of considering harmonics and corresponding diversity in modern power system loads, and validate the presented approach in introducing not only general types of loads, but also corresponding sub-types.

6.6.2 Harmonic attenuation

The effects of harmonic attenuation on the present and future aggregate load mixes are now briefly investigated. The ideal sinusoidal system voltage, which was applied to the considered load mixes in the previous section, is now replaced with the two distorted voltage waveforms: "typically distorted" and "heavily distorted", as defined in Section 2.12.2. The resulting harmonic content and associated diversity factors are shown in Figures 6.21 to 6.24.

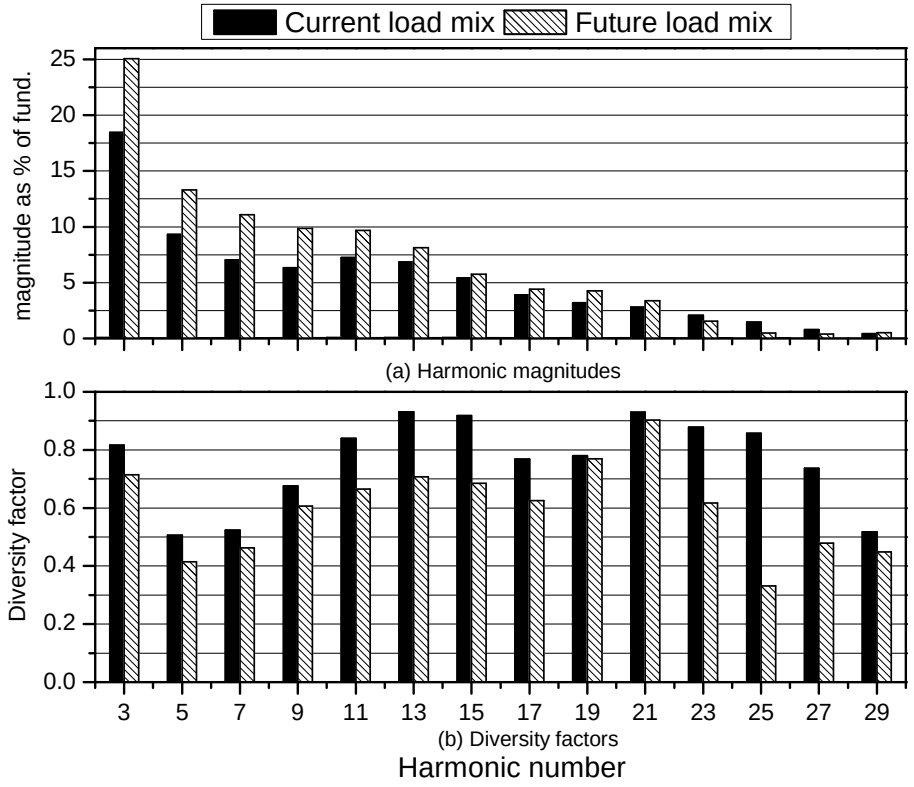


Figure 6.20: *Comparison between magnitudes and diversity factors of harmonics for present and future aggregate load mix.*

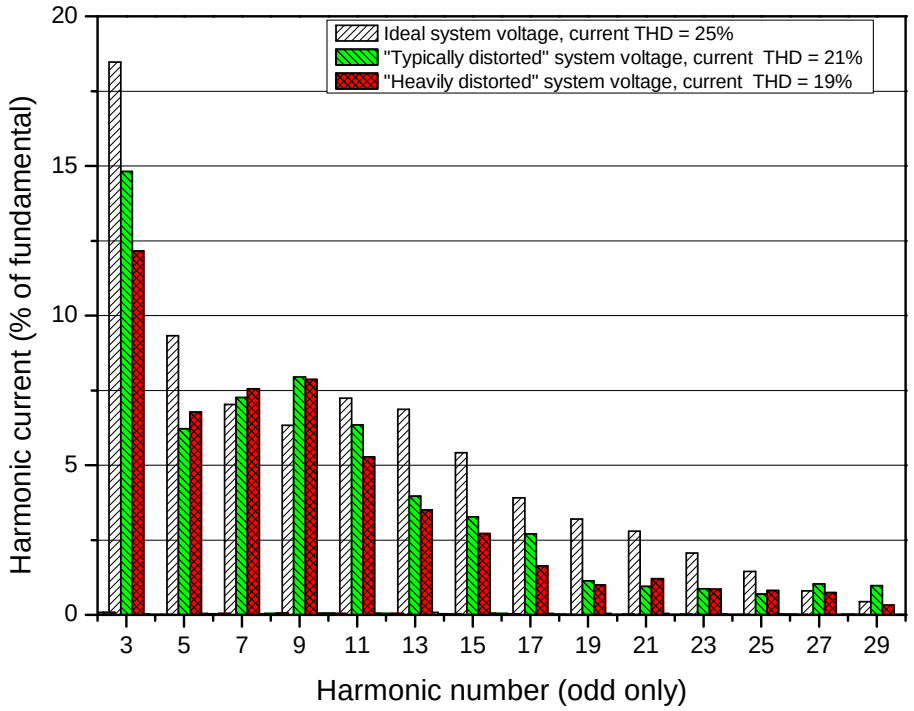


Figure 6.21: *Comparison of harmonic contents of present aggregate load mix with applied sinusoidal, "typically distorted" and "heavily distorted" system voltages.*

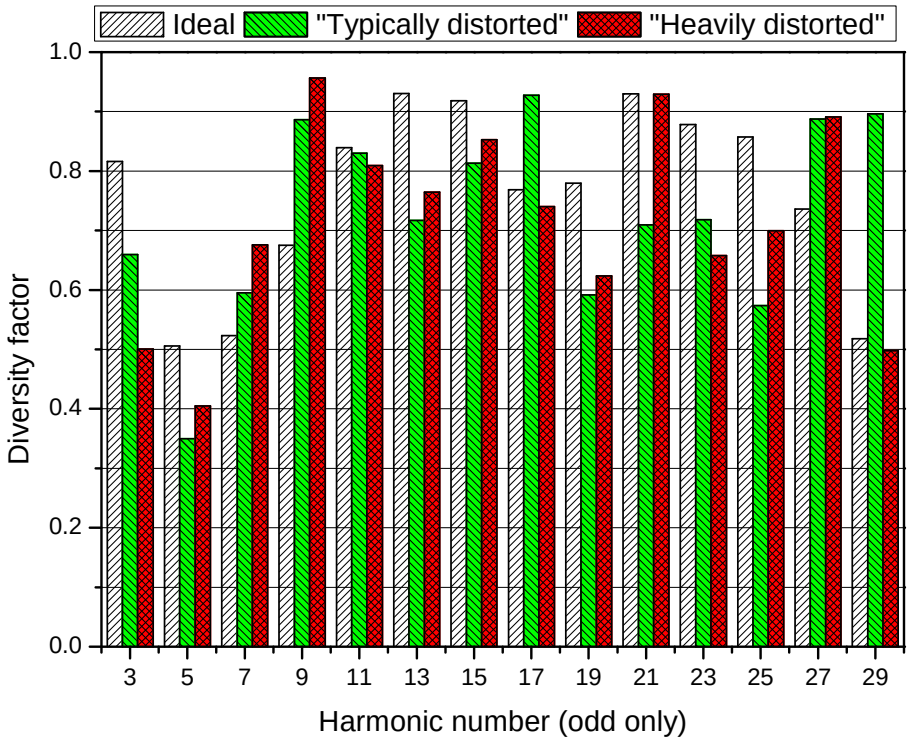


Figure 6.22: *Comparison of diversity factors of present aggregate load mix with applied sinusoidal, "typically distorted" and "heavily distorted" system voltages.*

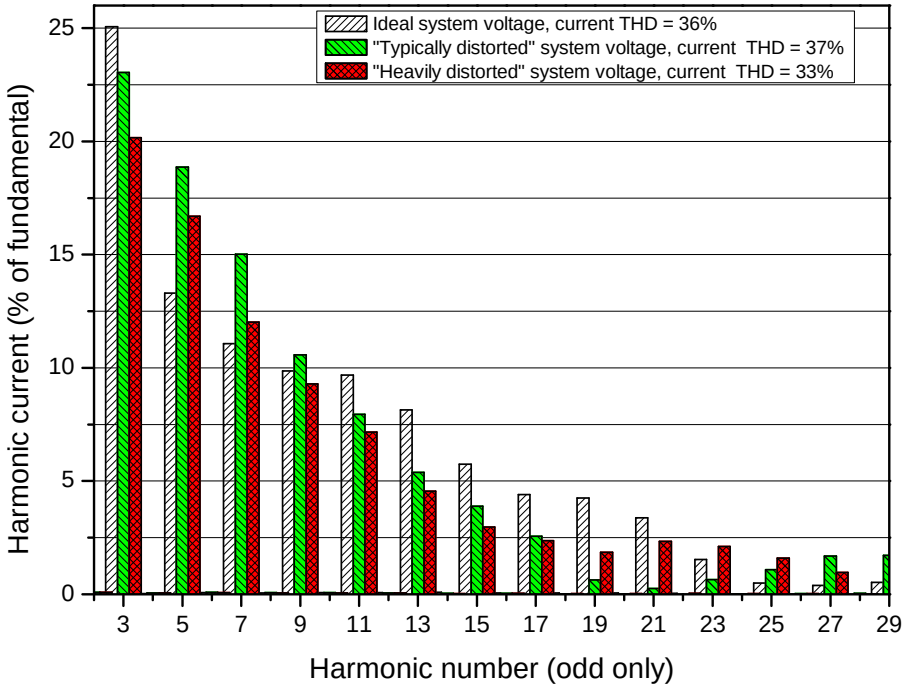


Figure 6.23: *Comparison of harmonic contents of future aggregate load mix with applied sinusoidal, "typically distorted" and "heavily distorted" system voltages.*

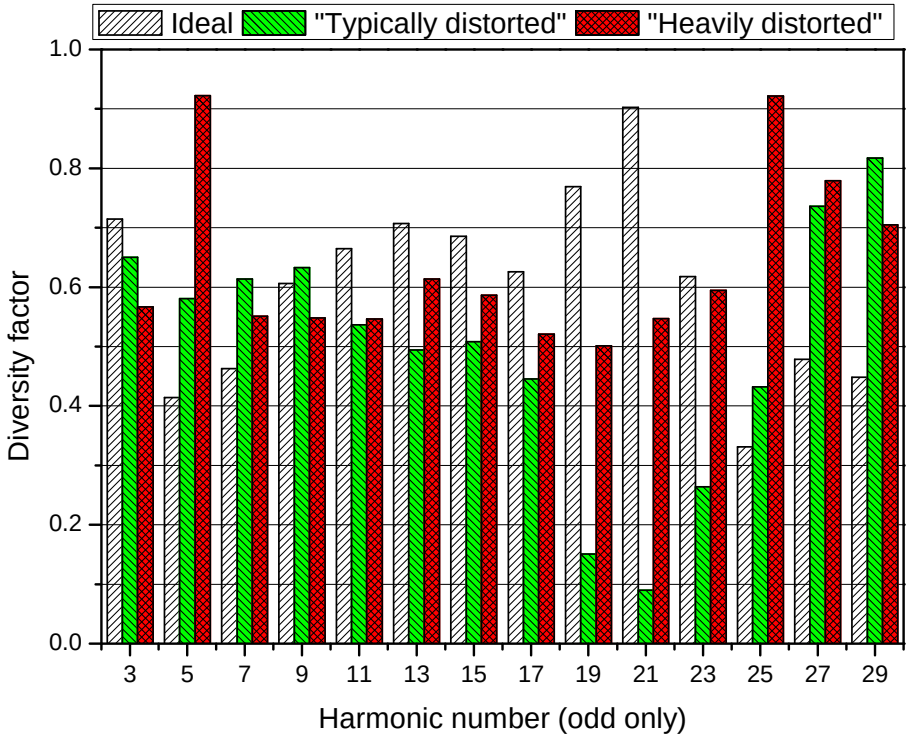


Figure 6.24: *Comparison of diversity factors of future aggregate load mix with applied sinusoidal, "typically distorted" and "heavily distorted" system voltages.*

The results presented in Figure 6.21 show that as the system voltage become more distorted, the THD of the aggregate load current waveform becomes less distorted. It can also be seen from Figure 6.21 that the 7^{th} and 9^{th} harmonics will be greater with applied distorted system voltage than in the case of ideal sinusoidal supply. The reason for this can be found from observing the diversity factors of the 7^{th} and 9^{th} harmonics as shown in Figure 6.22. The diversity factors of these harmonics are greater for distorted system voltage conditions than for sinusoidal ones. This is because distortion in system voltage will change both the magnitudes and phase angles of individual load type/sub-type harmonics. Accordingly, although the 7^{th} and 9^{th} harmonics of the individual loads types/sub-types will be lower in magnitude, there will be less cancellation between them, and hence their aggregate magnitude will be higher when compared to sinusoidal supply system conditions. Furthermore, it can be seen from Figure 6.22 that other harmonics will also have increased diversity factors for increased system voltage distortion, although the associated aggregate harmonic magnitude will not always be greater than the corresponding value for sinusoidal supply conditions. Therefore, a trade-off exists between amount of harmonic cancellation due to phase angle difference, and reduction in magnitude of the individual load type/sub-type harmonics.

The results presented in Figures 6.23 and 6.24 show similar effects of harmonic cancellation between individual load types/sub-types for three levels of system voltage distortion. It can be

seen from these results that the distortion of the future aggregate load mix aggregate current actually increases slightly with applied "typically distorted" system voltage, and decreases slightly for applied "heavily distorted" system voltage. This increase can be mainly attributed to the increase of 5^{th}, 7^{th} and 9^{th} harmonics. It was seen previously that the lower-power SASD, SMPS with no PFC and the CFL experience an increase of their harmonic content with applied "typically distorted" system voltage, and reduction with applied "heavily distorted" system voltage. Other non-linear loads tend to reduce their harmonic content with both "typically" and "heavily" distorted system voltage, with the exception of the ASD whose harmonic content is unaffected. As CFL and lower-power SASDs are more prominent in the future load mix, this explains why aggregate load current THD will increase with "typically distorted" system voltage and reduce with "heavily distorted" voltage.

From the presented results, it has been shown that the harmonic content of the considered aggregate system loads will not necessarily decrease with an increase of system voltage distortion, as is stated in much previous work. This is because the harmonic content of the aggregate load will be determined by the exact characteristics of the system voltage waveform i.e. not only its general shape (see Section 3.12.2 for further explanation). Thus, the particular load mix will have effect not only on the harmonic content of the aggregate load, but also on its characteristics when system voltage becomes distorted. This complex relationship between the actual characteristics of the modelled aggregate load and power supply system to which it is connected justifies and validates the general approach to load modelling adopted in this thesis.

6.7 Effect of non-linear load on supply system

The effects due to harmonic cancellation and attenuation on the aggregate present and future loads have been investigated and discussed in the previous sections. It is now interesting to consider these two effects together, and assess impact and extent of system-load interactions on a typical distribution system bus.

A simple two-bus system is considered in this example. MatLab and PSpice where used in order to apply the generic analytical models to a simple two-bus network, as this type of analysis is not possible in PSS/E, where only sinusoidal supply analysis (with polynomial and exponential models) can be performed. The development of this system-load interactive model is discussed below.

6.7.1 Simplified two-bus system model

In order to perform this investigation, it is necessary that the voltage supplied to the individual generic analytical models (which form the aggregate load model) is influenced (i.e. distorted)

by the (harmonic content of the) aggregate load it is supplying. Distortion of system voltage due to non-linear load occurs because the harmonic currents drawn by these loads lead to harmonic voltage drops in the supply system. The magnitude of each harmonic voltage drop will depend on the magnitude of the associated current harmonic and system impedance at the considered harmonic frequency. For the purposes of this example, a simple two bus system is considered, as shown in Figure 6.25. The system is a single-phase 230V supply, representing the closest point of common-coupling to considered load bus, (i.e. single-phase installation of the secondary of a typical 11/0.4kV distribution network transformer). The load bus is connected to the external supply system via the impedance, L_{sys} and R_{sys}. The value of this impedance is taken as typical for UK domestic distribution network, (i.e. Z = 0.25 + j0.23Ω), and in this example it also includes impedance of the external system, (see Section 1.8). The presented generic analytical model of the ASD is already implemented as a single-phase representation (see section 2.11) so no further modification of this model is required in order to apply it to the considered network. All other presented generic analytical models are single-phase and so can also be applied directly to considered network.

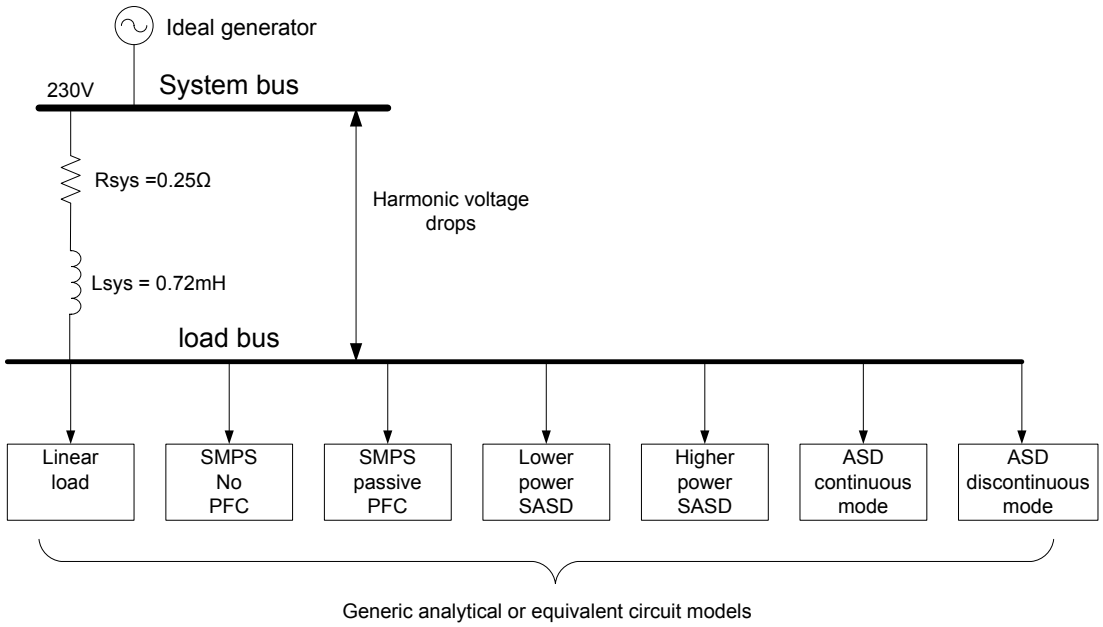


Figure 6.25: *Simple two-bus network used for analysis of voltage distortion due to non-linear load.*

The distortion of the system bus voltage due to applied non-linear loads is found by implementing the following iterative procedure in MatLab. Initially, the current harmonics of the considered aggregate load are obtained for applied sinusoidal voltage conditions. The obtained current harmonics are used in combination with the harmonic system impedance, to calculate the resulting harmonic voltage drops. The harmonic voltage drops are then subtracted from the system voltage, to produce a new, distorted load bus voltage. This new distorted

voltage is then applied to the aggregate load, and a new set of harmonic currents is obtained due to the effects of harmonic cancellation and attenuation. This process is repeated, until the THD values of the load bus voltage differs by less than 0.1% between the current and previous calculation. A flow diagram of this procedure is shown in Figure 6.26.

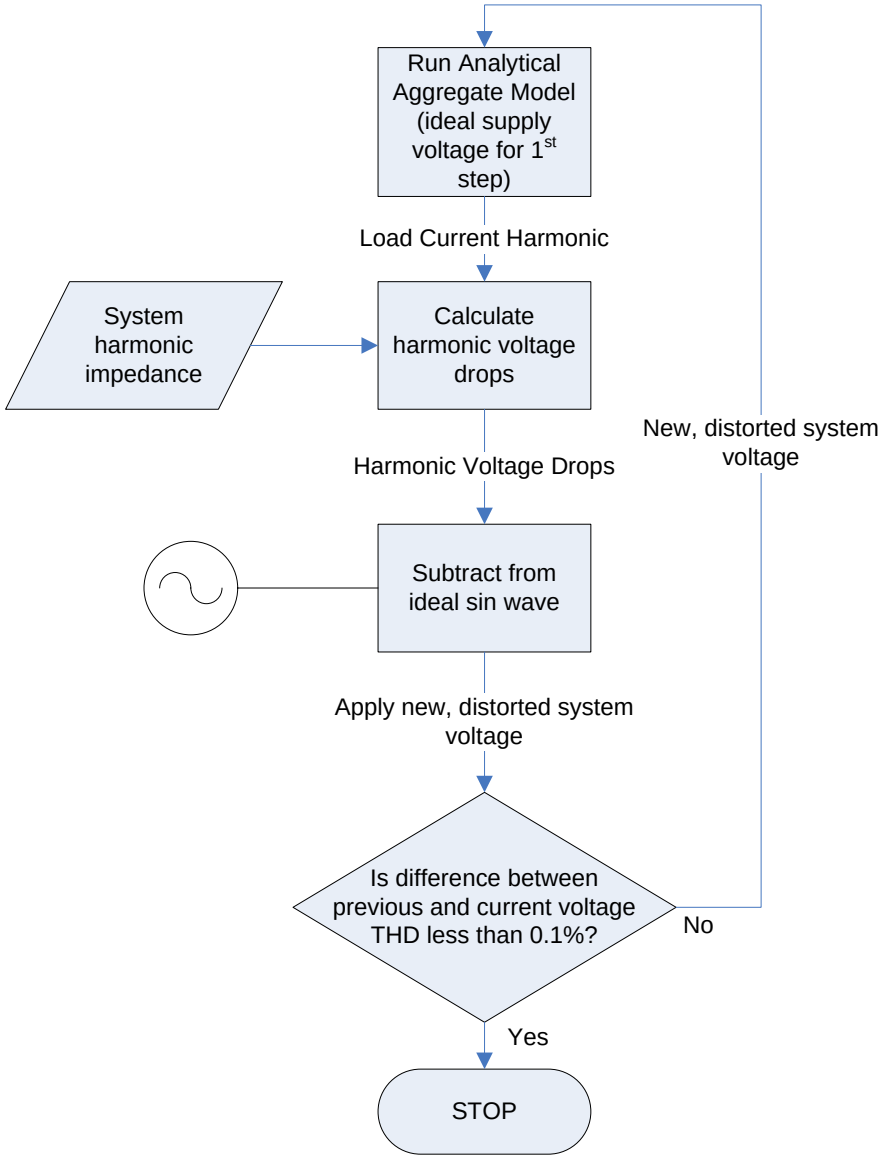


Figure 6.26: *Flow chart of applied procedure for the analysis of system voltage distortion due to non-linear loads.*

The discussed two-bus network may also be implemented directly in PSpice using the developed equivalent circuit models instead of the generic analytical models. When implementing the equivalent circuit models, some three-phase loads must also be connected to the load bus to represent the effect of industrial load in the considered load mixes. Connection of these loads to the proposed simple single-phase network is achieved by assuming that the

system is ideally balanced. Therefore, the load bus voltage waveform may be duplicated and phase shifted to represent the other phase voltages. By only considering the current in one phase of the three-phase supply, these loads can be effectively contributed to the single-phase aggregate current waveform. This process is not necessary in the case of generic analytical models of three-phase loads, as this is performed within the model, as described in Section 2.11.

6.7.2 Load bus voltage waveforms

The aggregate loads associated with the present and future load mixes were applied to the developed network models, both in MatLab and PSpice, in order to investigate their effects on load bus voltage distortion. The aggregate loads were both set to draw a nominal single-phase power of 5kVA. It should be noted that in a similar way, as discussed for the PSS/E network model, the exact value of system impedance and system loading are not important as the presented analysis is a comparative analysis designed to show the effects of change in future load characteristics on the supply system voltage and also to further verify developed models. Different values of system impedance and different loading on the system will merely exaggerate or reduce observed effects but it is the difference between present and future load mixes that are of primary interest.

Two scenarios were performed for each load mix. In the first scenario, the external system voltage is taken to be ideally sinusoidal, to represent an ideal external supply system. In the second scenario, the external system voltage is assumed to be "heavily distorted" (as introduced in Section 2.12.2), representing a system with high voltage THD. Problems were accounted with the MatLab code which failed to converge to a final solution especially for "heavily distorted" supply conditions. There was insufficient time available to resolve these problems and, therefore, the results of the analysis shown in Figures 6.27 and 6.28 are from PSpice model with applied equivalent circuit generic load models, which have the exact same characteristics as their analytical counterparts.

The results presented in Figure 6.27 show that the aggregate current of the present and future load mixes will lead to the familiar 'flat topping' of the load bus voltage. This provides further validation of developed load models, as the obtained simulated system load bus voltage waveforms are very similar to actual measured load bus waveforms (see Section 2.12.2). The load bus voltage THD is predicted to be 3.01% in 2020 compared to 2.21% currently, which is an increase of more than 35%. This is due to the increased harmonic content of the future load mix compared to the present load mix, as discussed in the previous sections.

The results presented in Figure 6.28, related to already distorted supply system voltage, predict that both the present and future load mixes will have similar, but less pronounced

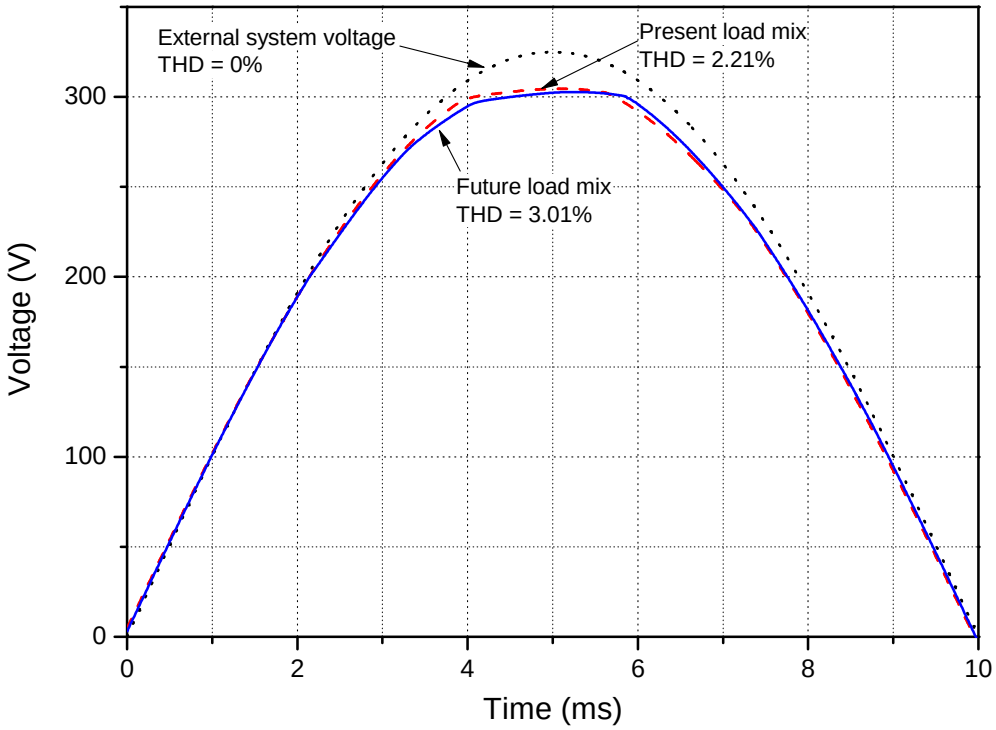


Figure 6.27: *Comparison of effects of present and future aggregate load mixes on typical domestic supply voltage (initial supply voltage ideally sinusoidal).*

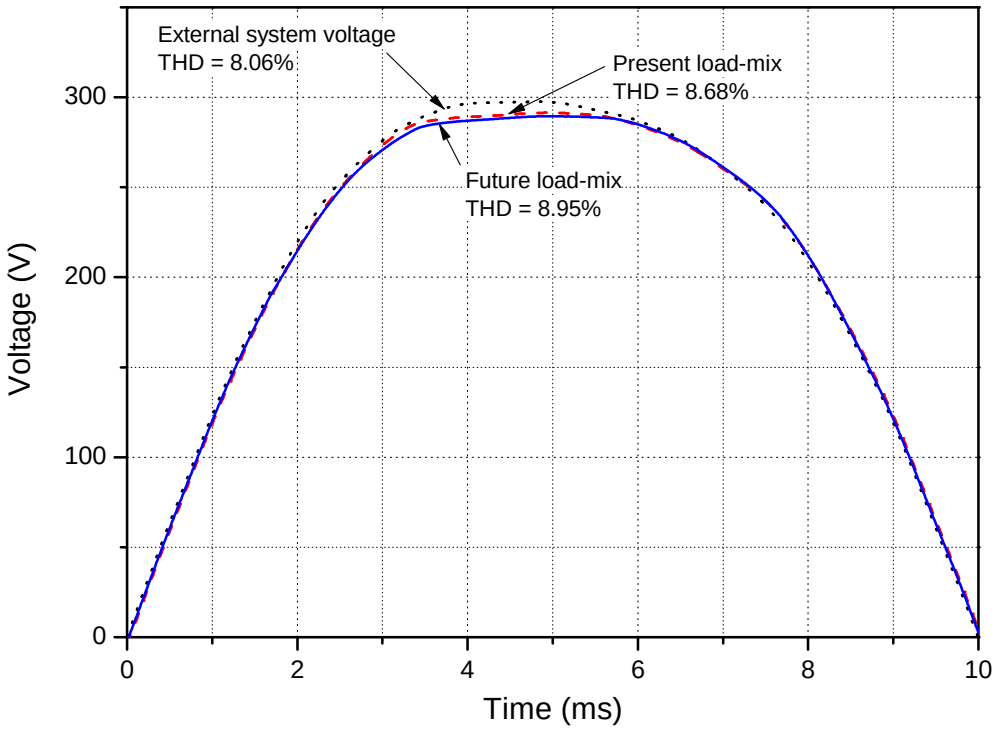


Figure 6.28: *Comparison of effects of present and future aggregate load mixes on typical domestic supply voltage (initial supply voltage already "heavily distorted").*

effects on the load bus voltage. The difference between the load bus voltage THDs is now only around 4%. This is because the external system voltage is already heavily distorted, and therefore the effects of harmonic content of the aggregate loads, due to the harmonic attenuation, are reduced compared to sinusoidal supply situations. This gives a good example of the interactions between the supply system and non-linear loads, and highlights further the importance of considering those interactions when performing harmonic analysis. It should be noted, however, that a starting system voltage THD of 8% is an extreme example.

The presented results demonstrate the ability of the proposed load models for a comprehensive and detailed analysis of the future (2020) typical distribution system voltages in urban areas.

6.8 Conclusions

This chapter has used the developed load models of individual types and sub-types of loads to form aggregate load models. In order to ensure that aggregate load models are representative of actual load in the system, a detailed review of available statistics has been performed. Accordingly, typical present and future load mixes for dominantly domestic load sector with a small amount of industrial sector load is established.

Methods of aggregation of the proposed and existing load models have been described in detail. Furthermore, the method of aggregation of the proposed generic analytical models has been verified by comparison of the results for aggregate load formed from these models with measured results for corresponding mixed load type aggregate. Aggregate loads were then formed using both proposed and existing individual load models for present and future load mixes. It was shown that aggregate loads formed from proposed load models have significantly different P-V, Q_1-V and PF_1-V characteristics from those formed from existing individual load models. The aggregate loads formed from proposed load models predict that the P-V characteristics of considered load sectors will become less sensitive to changes in system voltage in the future, while Q_1-V power demand characteristics will become more sensitive. The presented results also predict that the displacement power factor of considered aggregate load will improve due to the expected increased number of non-linear loads which operate at higher PF_1 and will replace linear loads. The presented analysis also showed that system voltage distortion will affect the displacement power factor of the aggregate load.

A model of a typical UK radial distribution system was used to investigate the effects of the different considered aggregate loads on performance of this network. This analysis further highlighted the differences between aggregate loads built from proposed and existing individual models. It was shown that the proposed aggregate load models predicted that in the future the considered system may allow for higher transmission of active power than currently, while

existing aggregate load models suggested the opposite would be true. The results of the analysis also indicated that distortion of the system voltage may have a fairly significant effect on load flow analysis, as distortion of the system voltage will cause reduction of fundamental reactive power demand of the considered aggregate load.

In order to further illustrate the strength and versatility of the developed models, they have been used to investigate the harmonic characteristics of the present and future load mixes. The presented analysis has highlighted some effects that different load types and sub-types may have on aggregate load harmonic content. In particular, it was shown that harmonic cancellation between different load sub-types, which have been caused by the introduction of harmonic legislation, is significant. These interactions have not been considered explicitly in previous work, where, for example, electronic loads have been taken as a single type of load and not further divided in sub-type loads. The presented analysis has also investigated the expected harmonic content of the future load mix, comparing it to harmonic content of the present load mix. It has been shown that in the future, aggregate load current is likely to be significantly more distorted than presently. This is due to two reasons: 1) the increased number and percentage contribution of non-linear loads, and 2) decreased numbers of linear loads, which will be substituted with non-linear loads. This increase in aggregate load current waveform THD, however, is less than what might be expected, as there is also increased harmonic cancellation in the future load mix. The increase in harmonic cancellation is due to the introduction of new and higher percentage contributions of non-linear loads.

Besides the investigation of harmonic cancellation, this chapter presented an investigation of harmonic attenuation. It was shown that in the present load mix, as supply system voltage becomes more distorted, the aggregate load current THD will reduce, which has also been reported in the previous literature and is an expected result. However, it is shown that for the future load mix distortion of the system voltage will have smaller effects on the harmonic content of the aggregate load. Furthermore, the presented results show that in "typically distorted" supply conditions the THD of the future aggregate load current waveform will actually increase by a small amount. This interesting effect was attributed to the increased contributions of lower-power SASDs, SMPS with no PFC and CFLs in the future aggregate load, and is a good subject for further research.

Finally, a simple two-bus system was developed in order to allow detailed analysis of load bus voltage distortion by applied non-linear loads. It was seen from these results that the present aggregate load mix distorted the load bus voltage in a very similar way to what was observed in measurements of actual system load buses. This important result provides further validation of the load models developed in this thesis. From this analysis, it was also found that the THD of the considered typical load bus voltage is expected to increase by approximately 35% in 2020 from the present value, for assumed ideally sinusoidal external system voltage. The similar

increase in voltage THD is much lower if the external system voltage is already distorted, due to e.g.propogation of harmonics from non-linear loads connected to adjacent feeders or parts of the network.

This chapter has demonstrated the flexibility of the developed load models, using examples to show how they may be used in multiple areas of power system analysis. It is further demonstrated that the proposed load models are not restricted to standard load flow analysis, as was the case in many previously developed load models. Furthermore, the presented analysis may be repeated with aggregate loads formed from desired or required load mixes, e.g. to represent daily, weekly or seasonal load variations, or to investigate different loads sectors, or to investigate the effects of single load types etc. Through the demonstration of the versatility of the developed model some other interesting results have also been produced. The most important (or most interesting) results indicate that harmonic and load flow analysis should not (necessarily) be considered as independent areas of research. A clear indicator of this is that aggregate load displacement power factor will be affected by system voltage distortion. Therefore, this chapter has clearly demonstrated the superiority of the proposed load models over the existing ones, and also identified important areas for further research.

Chapter 7
Conclusions and future work

7.1 Conclusions

Over the last few decades there have been significant changes to the way electrical energy is generated, supplied and consumed. This is due to a number of environmental, economical and social factors. In order to meet UK targets on the reduction of carbon emissions, there has been considerable investment in developing renewable forms of generation. Incorporation of this new type of generation into the existing power supply network has led to a number of challenges, and a need for a fundamental re-thinking of how best to operate power supply systems. This has resulted in increasing interest in (lower voltage) distribution networks, where distributed generation is often connected. In order to know how best to operate these networks and find best/optimal location for connecting these new forms of generation, it is important to develop representative and accurate models of distribution networks. This, however, also requires development of representative and accurate models of the load connected to the network.

The challenges presented by the need for the incorporation of a higher level of distributed generation are not the only reasons to invest time and effort into load modelling research. In the last few decades, the types and amounts of load connected to the supply system have also changed considerably, and are expected to change even more in the future. The last full review of component-based load models was carried out over twenty years ago. Accordingly, there is currently a lack of good/any models for many modern load types, that did not exist, or were not commonly used at the time of this last review. Additionally, the characteristics of the main load types considered over twenty years ago that are still in use today have changed over the years. This defines the overall aim of this thesis: To update existing component-based load models and establish new ones where necessary. In addition, as many of the considered loads are non-linear, developed load models should also be able to represent their typical non-linear characteristics.

7.1.1 Power electronic loads

The domestic sector has shown one of the largest changes in load inventory in recent years. The availability and affordability of (power) electronic devices has led to a large increase of

this type of load in private homes. This load type now represents a large proportion of the total energy consumed in the UK domestic sector (about 25%), with expected further increase by 2020 (to about 33%). Therefore, the characteristics of power electronic loads will have a significant effect on the overall/aggregate characteristics of the domestic load sector.

It has been shown in Chapter 4 that electronic load type will contain dc power supplies (also referred to as switch-mode power supplies ,SMPS, in this thesis), which may be further divided into three following load sub-types: 1) SMPS with no power factor correction (PFC); 2) SMPS with passive PFC, and 3) SMPS with active PFC. It has also been shown that the active power demand (P-V) characteristics of all these load sub-types are essentially constant with changes in system voltage, while their non-active power demand (N-V) characteristics will differ between each load sub-type. Several models of the electronic load type have been developed previously, but none of these has recognised that there are three distinctive sub-types of general dc power supply load. Furthermore, there was a disagreement between previously presented models. Reference [15] suggests that this load type has constant impedance P-V characteristics, [22] suggests that this load has close-to (but not) constant P-V characteristics, and [3] suggests that these loads have constant P-V characteristics. The work presented in this thesis clarifies these ambiguities, and shows that modern electronic loads will all have constant P-V power demand characteristics.

It has also been shown in Chapter 4 that present EU harmonic legislation ([30]) had a significant effect on the (N-V) and typical harmonic characteristics of modern dc power supply loads. This is because these loads, if rated above 75W, are required to have either passive of active PFC, in order to comply with EU harmonic legislation. There are at present no harmonic requirements for dc power supply loads with rated active power less than 75W. Therefore, these loads usually do not have any form of power factor correction.

The presented work has shown that the displacement power factor of dc power supply loads with rated power lower than 75W is typically close to unity (≈ 0.99) and "leading" (i.e. capacitive) for applied sinusoidal system voltage. However, on distortion of supply system voltage, these loads will become more capacitive with displacement power factor reducing to around 0.95 for heavily distorted conditions. These sub-types of load will also draw distorted current from the supply system, with THDs of around 210%, which will also vary with distortion in supply system voltage. On the other hand, dc power supply loads that have rated active power greater than 75W and use passive PFC will have displacement power factors (≈ 0.97) which shows little variation for applied sinusoidal or distorted supply conditions. They will be inductive ("lagging" PF_1) and will draw considerably less distorted current from the supply system (THD of about 100%) which will reduce with increased distortion in supply system voltage. Finally, dc power supply load containing active PFC circuits will operate with unity displacement power factor. The shape of their current waveform will match the shape of the supply system voltage,

i.e. it will be sinusoidal and in phase with voltage. In existing literature, load models of dc power supply loads are again in disagreement with regards to the representation of their displacement power factors. Reference [15] recommends that the power factor of these loads should be taken as 0.8, while reference [22] recommends that dc power supply loads are operated at unity power factor. Reference [3] does not make any recommendations. These references also do not make any comment on the value of displacement power factor under distorted system voltage conditions.

The fundamental reactive power demand (Q_1-V) characteristics of dc power supply loads with no PFC also differ from those of dc power supply loads with passive and active PFC. The Q_1-V characteristics of dc power supply loads with active PFC are not relevant, as their displacement power factor is unity. The Q_1-V characteristics of dc power supply loads with no PFC indicate that Q_1 demand will increase with an increase in system voltage. In electronic loads with passive PFC, Q_1 demand will decrease with increased system voltage. Once again, the Q_1-V characteristics identified previously are different. Reference [15] suggests that these characteristics change very significantly with change in system voltage. The other existing models either state displacement power factor is unity or do not discuss Q_1-V characteristics at all.

It can be concluded that Chapter 4 showed that modern dc power supply loads have considerably different active and non-active power demand characteristics to previously identified load models. These previous models are now outdated, and should not be used to represent modern electronic load type in system load models. It is also shown that the distortion in the system voltage will affect fundamental reactive power characteristics of dc power supply under 75W, which has not been considered in the previous work. It is also interesting to note that harmonic legislation had not only a significant influence on the harmonic characteristics of these loads, but also on their displacement power factor and Q_1-V power demand characteristics.

7.1.2 Single-phase directly connected and drive-controlled induction motors

Appliances that include single-phase induction motors are also common, making up a significant proportion of the total energy consumed in the UK domestic sector (around 26%) in 2008. These loads are usually classed as either “cold” or “wet” appliances, and include fridges, freezers, washing machines, etc. Until recently, directly connected single-phase motors (SPIM) have been commonly used in these applications. However, it is expected that in the future many of these motors will be replaced by single-phase drive-controlled induction motors (SASD), mainly due to the increased control and energy efficiency requirements. Chapter 3 investigated the characteristics of both directly connected and drive-controlled single-phase induction motors. The analysis showed that P-V characteristics of SPIMs are

to a great extend dependent on the type of SPIM and type of mechanical load the SPIM is driving (i.e. in what application SPIM is used). It was further shown that the reactive power demand (Q-V) characteristics of these linear loads are essentially independent of the type of motor mechanical loading. Previously presented load models of SPIMs are generally in good agreement with load models proposed in Chapter 3. This is to be expected, as the design of SPIM has not changed significantly in the last twenty years and, as they are linear loads, they have not been affected by harmonic legislation. The analysis of SASDs, however, showed that the P-V characteristics of these loads will be dependent on the type of drive control employed. If the simplest and cheapest form of drive control (V/Hz open-loop) is used, then P-V characteristics will depend on the type of mechanical load the motor is driving. If motor speed is regulated either by closed-loop V/Hz or advanced drive control techniques (e.g. vector control), then the P-V characteristics of these loads will be independent of the type of mechanical load the motor is driving.

The SASDs are non-linear loads, and will draw harmonic currents from the supply system. They will be, therefore, subjected to harmonic legislation. From the analysis presented in Chapter 3, it was shown that SASD with rated active power less than approximately 400W can comply with the present harmonic legislation without the need for any form of power factor correction. However, SASD with rated active power greater than 400W will need either passive or active PFC. Thus, there will be three following distinctive sub-types of SASD load: 1) those with no PFC, 2) those with passive PFC, and, 3) those with active PFC.

It was shown that the SASD with no PFC typically operates at high displacement power factors (≈ 0.99, for sinusoidal supply system voltage conditions), which reduces significantly to (≈ 0.93) for heavily distorted supply voltage. The SASD with no PFC is a capacitive load, drawing heavily distorted current from the supply system, with THD of around 190% for sinusoidal supply conditions (current THD will vary with distortion in supply system voltage). The SASD with passive PFC will typically operate at a much lower power factor (≈ 0.89), for both sinusoidal and distorted supply system voltage conditions. The SASD with passive PFC is an inductive load, and draws current with around 60% THD, which reduces with increased distortion in supply system voltage. The SASD with active PFC will operate in the same way as dc power supply loads with active PFC, i.e. with close to unity true power factor.

The Q_1-V characteristics of SASD with no PFC and with passive PFC will differ in characteristics, but, in a similar way to their P-V characteristics, this will depend on the type of drive control. For open-loop drive control, the Q_1-V characteristics will also depend on the type of motor mechanical loading. There are no previous load models of single-phase drive-controlled motors in existing literature, as these are relatively new devices. They are also expected to become more common over the next few years. From the analysis presented in Chapter 3, it is expected that these loads will have a significant effect on the characteristics

of the domestic load sector. Firstly, if SPIMs used in cold appliances, such as refrigerators and freezers, were replaced with SASDs with no PFC, there would be a considerable change in reactive power demand characteristics. This is because SASDs with no PFC operate at displacement power factors from 0.99 - 0.94 (depending on distortion in local system voltage), while SPIMs operate with much lower power factors (typically around 0.6-0.8). The effect of SASDs on P-V characteristics of typical domestic sector load will depend on the type of drive control employed in the SASDs.

7.1.3 Lighting loads

The last major load category in the domestic load sector which will exhibit major changes is lighting load. Historically, lighting load in the domestic sector has consisted mainly of incandescent lighting, which is a linear load. However, due to increasing concerns about energy consumption, this type of lighting is being phased out and replaced with compact fluorescent lighting (CFL). The CFLs are non-linear loads, and have different P-V characteristics to incandescent lighting. Chapter 5 has provided a review of this type of lighting load, discussing how modern compact fluorescent lighting will use electronic ballast to control the operation of the fluorescent tube. It was shown that CFL loads will have essentially constant current P-V characteristics. They are capacitive loads and typically operate with displacement power factors of 0.9 for sinusoidal supply voltage conditions, which reduces to around 0.82 for heavily distorted supply voltage. Being non-linear loads, they will draw distorted current from the supply system (THD $\approx$ 110% for sinusoidal supply conditions). As with other non-linear loads, current THD of CFLs will vary with supply system voltage distortion. These loads operate with such a low displacement power factors due to harmonic legislation, as in order to meet the legislation, small capacitors are used in CFLs ballasts. This has the effect of reducing the THD of the current drawn by the CFL, but also reduces its operating displacement power factor. There are several existing models of these loads, all of which correctly predict the P-V characteristics. Although these previous models were developed to represent linear fluorescent lighting (LFL), the characteristics of the fluorescent tube in both linear and compact fluorescent light sources are very similar, i.e. they operate as constant current loads. In existing models, however, there is a disagreement over the representation of the Q_1-V characteristics, for which a wide range of characteristics is suggested. This is also true for the displacement power factors of these loads. A few previous models simply do not suggest a value for this parameter. The work presented in Chapter 5 has clearly defined the characteristics of modern CFL lighting typically found in the domestic sector. As in the case of other considered loads (SASD and SMPS), CFL are also non-linear loads, and will therefore further increase the harmonics emissions in the supply system.

7.1.4 Three-phase directly connected and drive-controlled induction motors

Significant changes to load characteristics in the past few decades have not only occurred in the domestic sector. There has been a significant shift towards the use of drive-controlled three-phase motors in various applications in the industrial sector, where previously only directly connected three-phase motors were used. Three-phase drive-controlled motors are non-linear loads and have very different characteristics to directly connected motors. Chapter 2 has presented an analysis of the steady state active/non-active power demand characteristics of three-phase directly connected and drive-controlled induction motors. It has been shown that there is a clear distinction between active power demand characteristics of lower-power ($\leq$ 15kW) and higher-power (15kW-160kW) directly connected motors. This is because P-V characteristics of lower-power motors are strongly influenced by the type of motor mechanical loading, i.e. by the application in which the motor is used. The Q-V characteristics of both higher-power and lower-power motors were shown to be similar and independent of the type of motor mechanical load. Proposed exponential and polynomial models of lower and higher-power directly connected motors have been compared with the existing models, where available, and have been found to be generally in good agreement.

From the presented analysis, it was also shown that currently common V/Hz controlled open-loop ASDs will have similar P-V characteristics to corresponding lower-power or higher-power directly connected three-phase motors. However, ASDs that employ V/Hz closed-loop control, or have advanced control, will have P-V characteristics that are independent on motor mechanical loading condition. The N-V characteristics of ASDs have been shown to be influenced by the type of mechanical loading, the values of dc link components and, to a lesser extent, system impedance. Based on the values of dc link components, ASDs will operate in either continuous or discontinuous mode. Each mode of operation results in significantly different N-V and harmonic characteristics. Therefore, in addition to being divided/classified by rated power, ASD load type should also be divided into continuous and discontinuous current mode load sub-types. The ASDs operated in continuous mode will have typical displacement power factors of 0.99, which are unaffected by system voltage distortion. They act as inductive loads and will draw current from the supply system with THD of approximately 40%, which is again unaffected by distortion of supply system voltage. The ASDs operated in discontinuous mode will typically have power factors of 0.98. They will also operate as inductive loads and draw current with THD approximately 90% from the supply system. Again both PF_1 and THD of this load sub-type will be unaffected by the presence of distortions in the system voltage.

In this thesis, it was also concluded that the design of ASD load will not be directly influenced by harmonic legislation, which is in contrast to the other non-linear loads considered in this work. There are only two existing models of ASD, both related to lower-power ASD, presented

in [22]. These previously presented models are in disagreement with the proposed models, and there is a significant doubt about their accuracy.

The work in Chapter 2 has presented new load models for ASDs and confirmed that existing load models of directly connected three-phase motors are generally still valid. However, care should be taken when considering lower-power directly connected motor loads, as the type of applications where the motors are used will have a significant effect on the P-V characteristics of this load type. It is also of importance to note that ASDs operated in both continuous and discontinuous modes have close to unity displacement power factors, and will therefore not contribute significantly to reactive power flow in the supply system. If these drives are used to replace directly connected three-phase motors with typical power factors of, 0.8-0.9, there will be a large reduction in the demand for reactive power flow in the supply system. The other main issue in relation to increased amount of ASD loads is increase of harmonics in the supply system, which will have adverse effects on system voltage quality.

7.1.5 Generic load models and aggregation of individual load models

In each "load" chapter, generic equivalent circuit models and analytical models of considered load types and sub-types were proposed, including their typical P-V, N-V and harmonic characteristics. These generic load models may be used to form aggregate loads for further investigation of P-V, N-V characteristics at bulk supply points. They may also be used for the investigation of harmonic interactions between the system and different load types and sub-types.

The proposed generic analytical models of individual loads are aggregated in Chapter 6, to form present and (expected) future aggregate loads. Considerable effort was invested in establishing these present and future load mixes, which in the considered example consist of 80% domestic sector load and 20% industrial load. The proposed aggregate loads show that in the future the P-V characteristics of typical domestic and industrial load are likely to become closer to constant power load type, with Q-V characteristic becoming closer to constant current load type. Also, load displacement power factor of aggregate load is likely to improve significantly in the future. The previously presented load models, (Table 1.1, [9], [15], [17] and [18]) were also aggregated for considered present and future load mixes. These models, in contrast to the proposed models, suggest that in the future there will be little change to aggregate load P-V and Q -V characteristics. They also wrongly predict that displacement power factor will decrease.

In order to better compare the proposed aggregate load models with the existing load models, they were applied to a typical UK distribution network. Constant MVA, constant current and constant impedance load models were also considered. Constant MVA load models are most commonly used as a "worst-case" load model, where constant current load, according to [26],

is often considered as a more realistic representation of aggregate system load.

The results of the analysis showed that the load meeting capacity (LMC) of the considered example network was lowest when the load was assumed to be constant MVA, and greatest for assumed constant impedance load, for both present and future load mixes, as would be expected. The results also showed that for the present load mix the proposed aggregate load models predict a lower LMC than the aggregate load model formed from existing load components. Conversely, in the future, the proposed aggregate load models predicts higher network LMC than the aggregate load model formed from existing load components. It was also shown that reduction in displacement power factor due to distortion in the supply system voltage is likely to increase the actual network LMC. The results also showed that even though the proposed future load is predicted to have more of a constant P-V characteristic, than presently, it will demand far less reactive power and therefore the LMC of the considered network will actually increase.

The main focus of this thesis was not network analysis and therefore the presented analysis is simple (due to time restraints). Nevertheless the presented analysis was used to highlight the significant shift in aggregate load characteristics since the 1980s. It further shows that significant error in prediction of network LMC is likely to occur, if older load models are assumed, which could have serious implications on network planning, design and operation. The shift in characteristics of load models is also expected to have significant influence on other factors such as optimal location, size and financial feasibility of distributed generation (DG). Finally, the effect of system voltage distortion on reactive power demand of the aggregate load may also significantly affect network analysis and DG placement, and both of these areas are suggested for further research.

7.1.6 Harmonic content of aggregate load

The harmonic characteristics of present and future load mixes were investigated using proposed generic load models. It was found that diversity in non-linear loads will have a major influence on the harmonic characteristics of both present and future load mixes. This is a significant finding, as much diversity in non-linear loads is due to harmonic legislation introduced in 2001. This diversity has not been considered in the previous work. The most interesting harmonic cancellation can be observed between electronic loads with passive PFC and electronic loads with no PFC. It is expected that electronic loads with no PFC will dominate in the harmonic contents of the present and future loads, as the input current THD of these loads is high compared to all other non-linear loads. However, the harmonic content of lower-power SASD load is also very high, and as these loads are expected to replace some very common loads, such as refrigerators, they are expected to have a significant influence on supply system harmonic

content in the future. In the presented example, a fairly conservative value of 25% of predicted SPIM load to be replaced with lower-power SASD in the future load mix was selected, but even this small figure had significant effect on harmonic content of aggregate load. It is interesting to note that dc power supply loads (over 75W) must meet stringent Class D harmonic limits,where as, SASDs must meet less stringent Class A limits irrespective of rated power. This may be an oversight in current harmonic legislation, which does not recognise the potential impact of a large increase of this load type on system performance/voltage quality.

The estimated present and future aggregate load mixes were applied to a representation of a "typical" domestic system bus, and the influence of these loads on supply voltage distortion investigated. It was shown that in the future the typical bus voltage is expected to be more distorted than in the present. As discussed previously, this has implications on reactive power demand, as well as implications on future harmonic legislation, which is likely to be adjusted to reduce voltage THD at the load bus. Harmonic legislation relevant to all load models developed in this thesis should be monitored in the future, as any changes are likely to affect active power and non-active power demand characteristics, as well as harmonic characteristics, of modern power system non-linear loads. Investigations into the likely effects of future changes in harmonic legislation are, therefore, an important area of further/ongoing research.

7.1.7 More general discussions

This thesis has taken a different approach to load modelling than (any) other previous work in this area. The main difference in the selected approach is that it does not make the assumption that the harmonic content of power system load is independent from the analysis of reactive power and power factor, which is usually assumed in standard load flow analysis. This approach has been facilitated by the recent clarification of the definitions of active and non-active power quantities that should be used for the analysis of non-sinusoidal voltages and currents, [38].

Accordingly, the presented load models take into account all harmonic characteristics, as well as P-V and N-V characteristics, of considered load types, by reproducing the actual current waveform of the considered aggregate load. This makes the developed load models extremely flexible as practically all important information is preserved if current and voltage waveforms are available. This flexibility is combined in this thesis with the fact that the major type/sub-types of present and future loads have been identified and modelled. Based on that a comprehensive library of load models is formed, which then can be used directly in different areas of research, especially if there is current uncertainty about load models. Two examples of the more general use of developed load models are now briefly discussed.

As any desired aggregate load mix may be created from the developed library of load models, this can be used for detailed investigation of any of the major load sectors, as

well as for investigation of expected future changes load characteristics. The incorporated ability to investigate characteristics of future loads is a very important and powerful feature, as measurement-based approaches simply can not be used to achieve this. However, the developed models are not proposed as a substitute to measurement-based models, but to complement them. This is because the developed models predict the actual shape of the aggregate current waveform, which is built from individual loads, and the process may be reversed, and load mix can be established from the measured aggregate load waveforms. Once the actual load mix at a particular bus is established, it may be used as the basis to predict the change of future characteristics of this load.

An area of research receiving greater attention in the last years is demand side management (DSM). This concept involves control or disconnection of individual loads, such as refrigerators and freezers, from the supply to balance load flow. In order to fully ascertain the effect of DSM on the supply system, it is necessary to have aggregate load models that allow for manageable loads in the aggregate mix to be connected or disconnected as desired. Therefore, the proposed load models are ideally suited for this task.

Finally, the work in this thesis has shown conclusively that the fundamental reactive power consumption of both present and future aggregate loads will be affected by the distortions in the supply system voltage. This effect is not significant at present, but it will increase with both percentage contribution of non-linear loads and level of distortion present in the system voltage. Therefore, relatively large error may be introduced to standard load flow analysis, if assumption of ideally sinusoidal operating conditions is made. The exact level of this error, however, should be further investigated for different operating and loading conditions.

7.2 Further work

This section suggests some areas of further work, directly related to the results of the research presented in this thesis:

1) The presented work has shown that harmonic legislation will have a significant influence on N-V and harmonic characteristics of aggregate loads. Therefore, any changes in this legislation are likely to have again a large influence on the characteristics of both individual and aggregate loads. This effect, obviously, should be quantified for expected or anticipated changes in harmonic legislation. In order to achieve this, a comparative analysis of harmonic content at a typical load bus with current EU harmonic limits, and harmonic content with expected changes (e.g. the reduction of the Class D limits from 75W to 50W) should be performed. Similarly, other suggested changes, e.g. inclusion of lower-power SASD load in Class D limits, should be investigated. This analysis should focus on the domestic load sector, and can be performed for a variety of load mixes to represent daily/weekly/seasonal variations in load and demand structure. A network model able to consider both load flow and current harmonics, that allows for system bus voltage to become distorted, should also be developed to facilitate this research. This model may also be used to quantify more accurately the error of assuming sinusoidal system voltage in power flow analysis.

2) The effects of diversity within aggregate loads of the same type and sub-type should be investigated further. This investigation can establish the expected level of harmonic cancellation obtained during the aggregation of same type/sub-type loads. As previous work in this area has only considered SMPS with no PFC, inclusion of other loads types/sub-types is a logical way to improve this research.

3) In the future, electric vehicle battery chargers are expected to become a common load type. They will draw significant power and presently there is no available accurate load model for this load type. It is suspected that they will be SMPS loads, but the harmonic limits relevant to this loads are at present unclear. Accordingly, research should be performed to ascertain the likely topologies of these loads, and from this information corresponding generic load models should be developed. After that, the developed load models of this load type may be used with models of other loads developed in this thesis to investigate the likely effects of this new load type on aggregate load characteristics and system operation.

4) LED lighting is expected to become popular in the future, and this load has not been considered in this thesis. The considered profound effect of wholesale substitution of incandescent lighting with CFLs may also occur if LEDs are used for replacing CFLs, at least from the point of view of reduced active power. Therefore, accurate load models should be developed for LED lighting.

5) It should be investigated whether it is possible to identify likely load mix of a given bus from its measured current waveform. The generic analytical model can form the basis of an algorithm that identifies specific load 'signatures' in the aggregate current waveform. Once the method is working, it may be used to rapidly predict load mix for a number of measured buses, and these results compared with bus load mixes identified from statistical measurement-based approaches.

6) It was shown in [35] that the developed SMPS model can be used directly for the analysis of 'inrush current'. Therefore, this model is a transient model, as in simulation, steady-state characteristics are obtained after waiting for energising transient to finish. It is expected that the other developed non-linear load models, as of similar form to the SMPS model, may also be used as transient models, although they may need some minor modifications. This should be confirmed in further research by comparisons of models with measurements or with developed full circuit models of relevant load type/sub-type. Once it has been established that the developed load models in this thesis are indeed transient models they may be used in transient analysis, which will significantly extend the usefulness of the developed load models.

7) The developed load models may be used directly to investigate the effects and viability of demand side management on the supply system. This can be achieved by disconnecting and connecting selected 'manageable' individual loads based on an indicator such as magnitude of local supply system voltage or system frequency. The developed load models are ideally suited to this task. From the previous point the analysis may also be extended to include likely transient effects of DSM on the supply system.

8) The presented load models may also be used to investigate the effects on design, planning, placement and feasibility of incorporating new DG. Reference [2], has performed a similar analysis but compared constant MVA model with a supposedly more accurate exponential model. The models presented in this thesis allow for a far more in-depth analysis, that takes into account harmonic as well as standard power flow quantities (i.e. P and Q) which have been shown in this thesis not to be independent.

9) The introduction of any new load types should be followed by the corresponding development of new load models using the procedures outlined in this thesis and then the load library updated accordingly, (see points 3 and 4).

Appendix A

A.1 PSpice model of three-phase dq motor

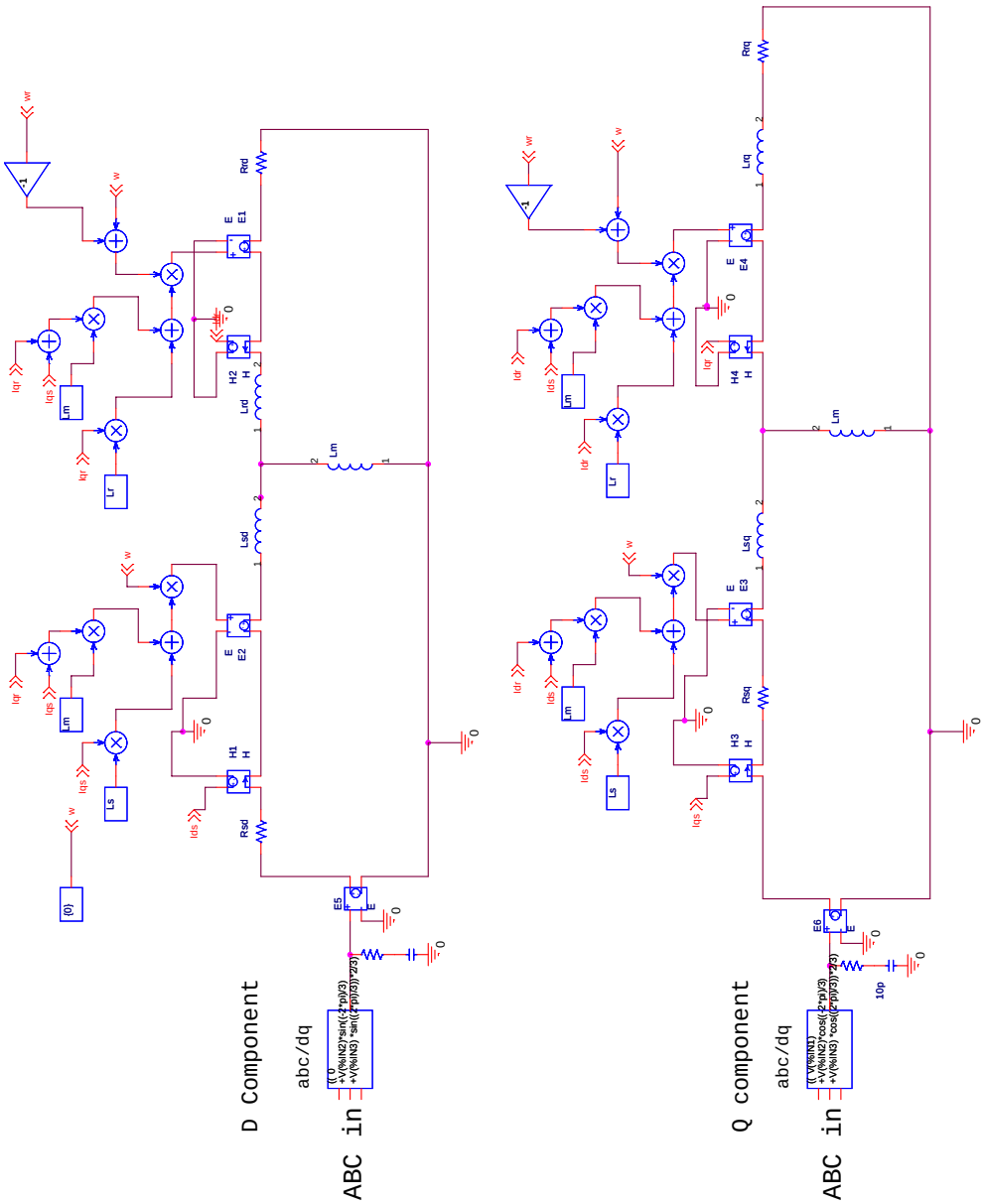


Figure A.1: *PSpice schematic of dq motor with ABC/dq interface.*

A.1.1 PSpice motor mechanical model

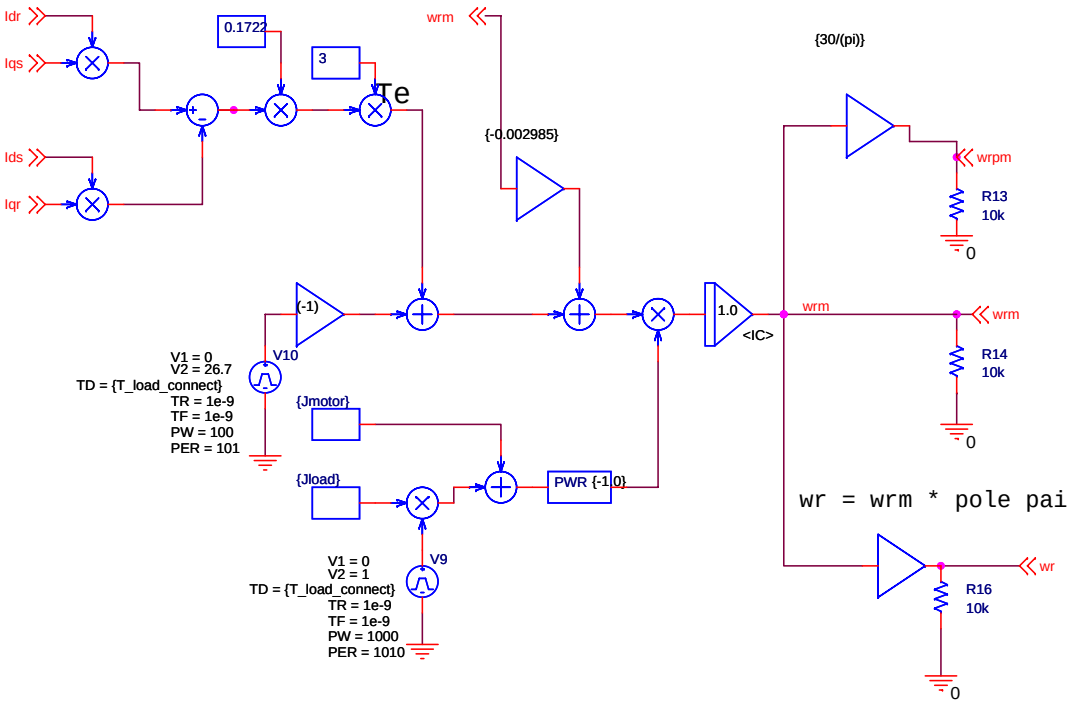


Figure A.2: *PSpice schematic of three-phase motor mechanical model.*

A.2 V/Hz ASD

A.2.1 V/Hz controller

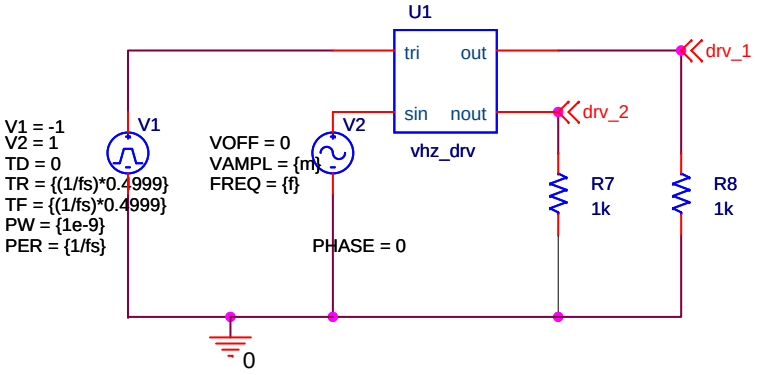


Figure A.3: *V/Hz controller.*

A.2.2 PSpice model of three-phase motor drive

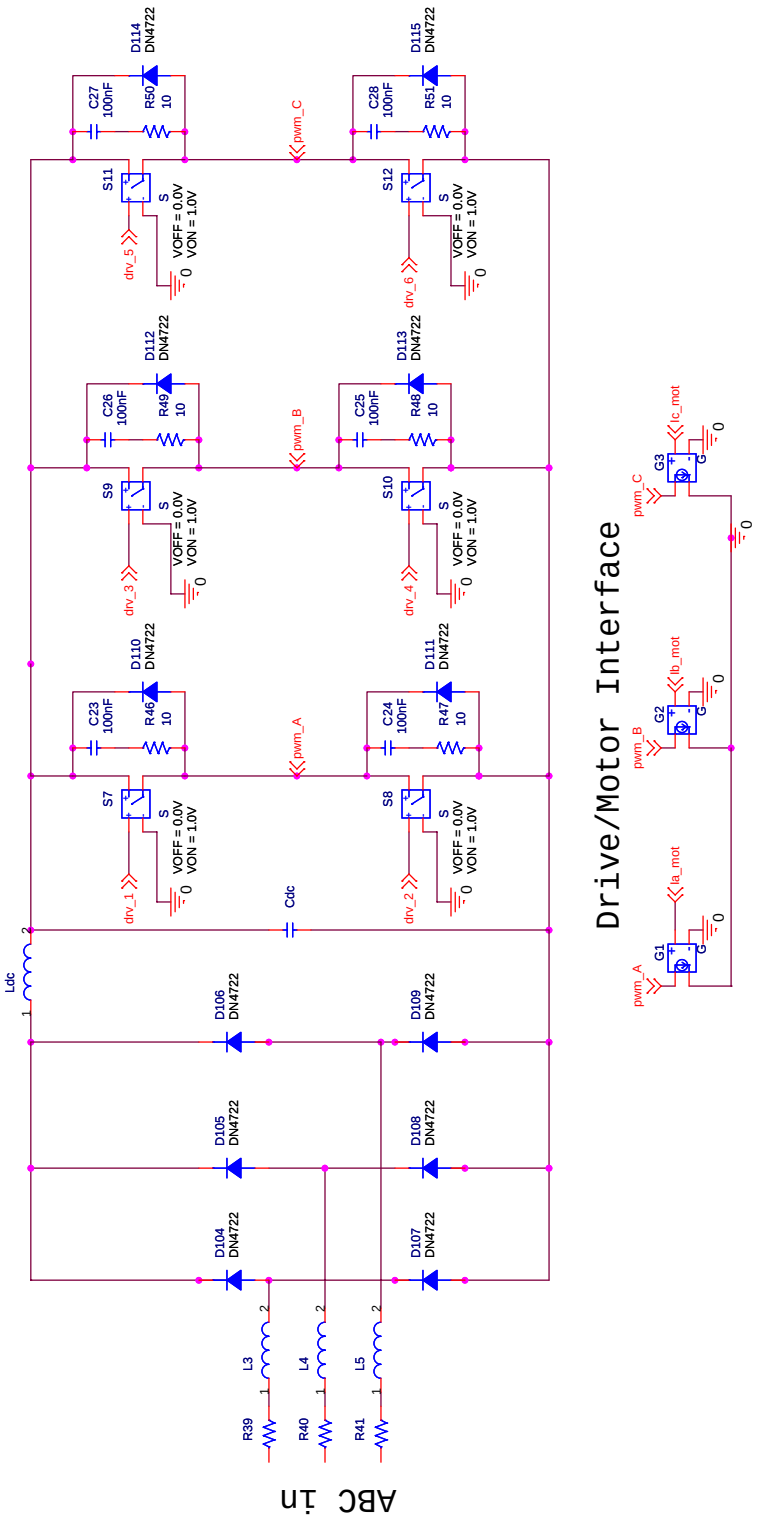


Figure A.4: *PSpice schematic of three-phase motor drive.*

A.3 Validation of ASD equivalent circuit model, for linear torque, quadratic torque and constant mechanical power loading conditions

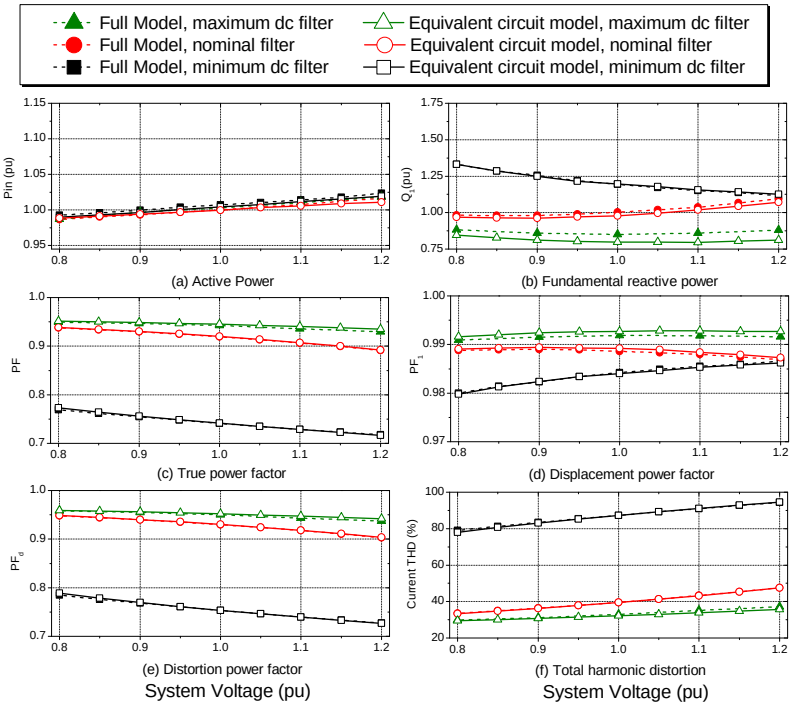


Figure A.5: *Comparison between full and equivalent ASD for a range of dc link component values and motor loaded with linear torque load.*

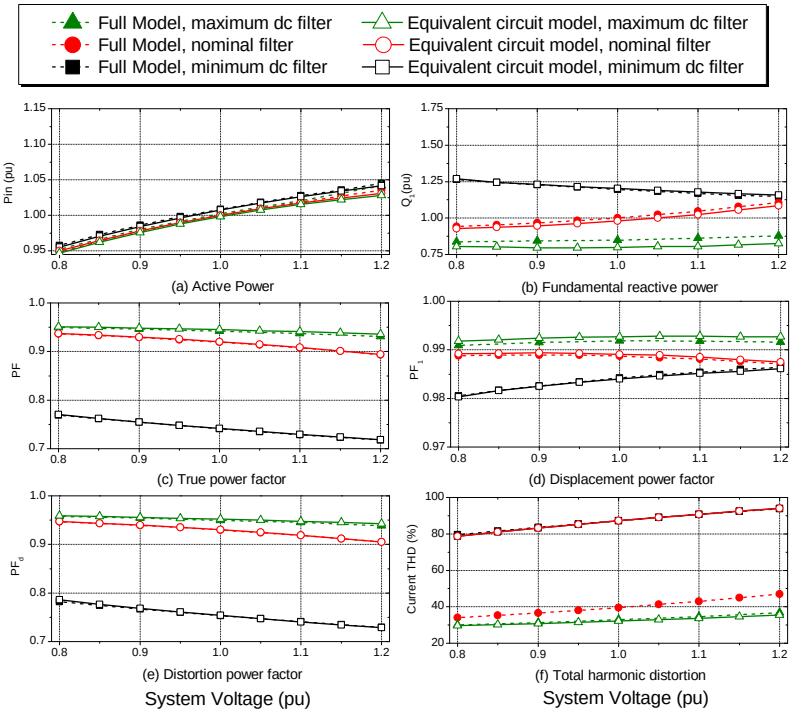


Figure A.6: *Comparison between full and equivalent ASD for a range of dc link component values and motor loaded with quadratic torque load.*

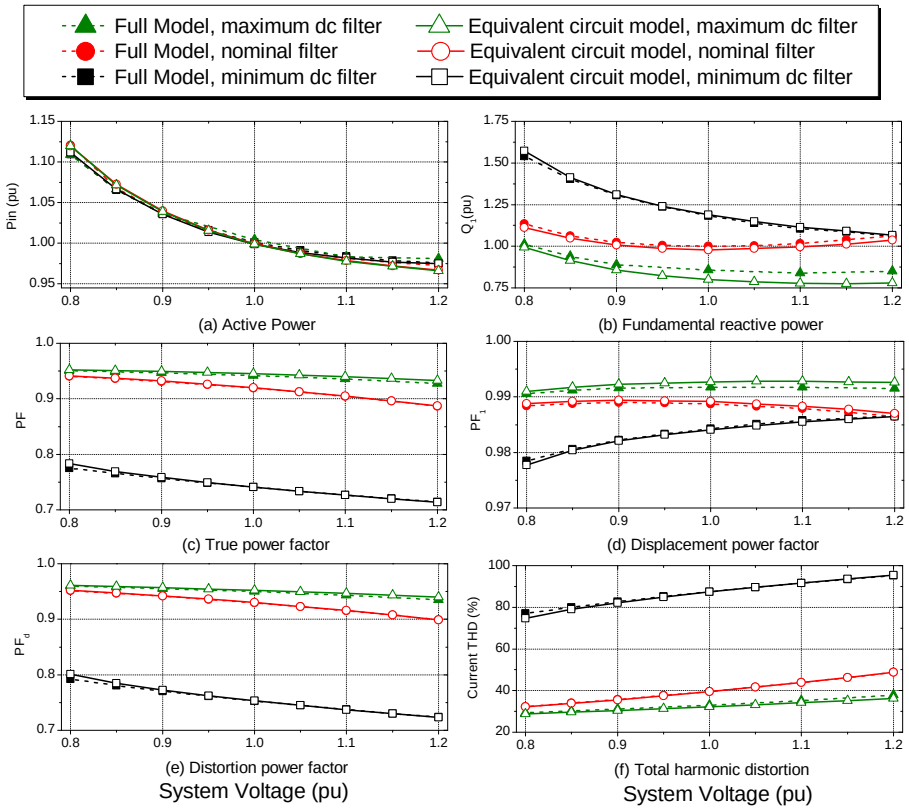


Figure A.7: *Comparison between full and equivalent ASD for a range of dc link component values and motor loaded with constant power mechanical load.*

A.4 MatLab code for three-phase ASD equivalent-analytical model

A.4.0.1 Decide on conduction mode

```
%Decides wther in continious or dis mode
%set initial value of M
vdc_rms = E; %set initial values of Vdc_rms.
M = (vdc_rms*vdc_rms)/P_rated;
L = (Lsys*2)+ Lfilter; %total L for continuous mode
%first run with no commutation taken into account
[t, iv] = solvediff_three_phase(0,(300e-3),V_int,C,L,Lsys,R,M,w,E,ts,0..
..,mag,angle_rad,no_of_harms);
vdc_rms = sqrt(mean((iv(round(length(iv)-20e-3/ts):length(iv),2).*..
..(iv(round(length(iv)-20e-3/ts):length(iv),2)))));
M_new = (vdc_rms*vdc_rms)/P_rated;
%take commutation into account
duration_com = 0.11e-3; %inital guess
V_int = iv(length(iv),2);
```

```
I_int = iv(length(iv),1);
loop_no =1;
%run loop,
while loop_no < 300
%first no-commutation period Lsys = 2*Lsys
L = (Lsys*2)+ Lfilter;
[t_noncom_1, iv_noncom_1] = solvediff_three_phase(0,(1/50)/12, V_int,C,..
..L,Lsys,R*2,M_new,w,E,ts,I_int,mag,angle_rad,no_of_harms);
%communtation period Lsys = 1.5*Lsys, R =
L = (Lsys*1.5)+ Lfilter;
V_int = iv_noncom_1(length(iv_noncom_1),2);
I_int = iv_noncom_1(length(iv_noncom_1),1);
[t_com, iv_com] = solvediff_three_phase_con_commutation((1/50)/12 -ts,..
..((1/50)/12+duration_com), V_int,C,L,Lsys,R*1.5,M_new,w,E,ts,I_int,..
..mag,angle_rad,no_of_harms);
%finish off cycle with noncom mode
V_int = iv_com(length(iv_com),2);
I_int = iv_com(length(iv_com),1);
L = (Lsys*2)+ Lfilter;
[t_noncom_2, iv_noncom_2] = solvediff_three_phase(((1/50)/12)+..
..duration_com-ts,(2/50)/12, V_int,C,L,Lsys,R*2,M_new,w,E,ts,I_int,mag..
..,angle_rad,no_of_harms);
%put waveform together
iv_new = [iv_noncom_1;iv_com(3:length(iv_com),:);..
    ..iv_noncom_2(3:length(iv_noncom_2),:)];
t_new = [t_noncom_1;t_com(3:length(iv_com),:);..
    ..t_noncom_2(3:length(iv_noncom_2),:)];
V_int = iv_new(length(iv_new),2);
I_int = iv_new(length(iv_new),1);
%Now want to update t_com so vo is the commutation vrect:
start_com = (1/50)/12;
%distirt code already takes phase shift and amplitude into account
vdc_set = distorted_sin_asd(mag,angle_rad,start_com,no_of_harms);
col=1;
I_charge = 0;
t_charge = ts;
%this sets the charging current
 %while the phase current is less than the dc link current
while I_charge(col,1) < iv_new(col+round(start_com/ts),1)
col = col + 1;
t_charge = t_charge + ts;
iv_new(col+round(start_com/ts),1);
vin = distorted_sin_asd(mag,angle_rad,t_new(col+round(start_com/ts)),..
..no_of_harms);
vo = vin - vdc_set; %voltage inductor resistor series circuit 'sees'
 %RL charging equation
I_charge(col,1) = (vo/R*2)*(1 - exp(-t_charge/(Lsys*2/R*2)));
duration_com = col*ts;
```

```
end

%now update M;
vdc_rms = sqrt(mean(iv_new(:,2).*iv_new(:,2)));
M_new = (vdc_rms*vdc_rms)/P_rated;
loop_no = loop_no +1;
end
%clear old varaibles
iv=[];
t=[];
%this put iv into half cycle ifilter waveforms
iv = [iv_new; iv_new(1:length(iv_new),:); iv_new(1:length(iv_new),:)];
t = 0:ts:0.01-4*ts;
t=t';
col = 1;
dis_con_flag = 0; %set flag
%look for dicon mode
while col < length(iv)
if iv(col,1) < 0
    dis_con_flag = 1
    break
else
    col = col + 1;
end
end
if dis_con_flag ==1 %if in discontinuous mode
 [data_out] = discontinuous(C,Lfilter,Lsys,R,w,E,ts,Vsys,P_rated,..
 ..mag,angle_rad,no_of_harms);
else %if in continuous mode
    [data_out] = continuous(iv,Lsys,R,w,E,ts,Vsys,vdc_set,I_charge,..
    ..start_com,t_new,mag,angle_rad,no_of_harms);
end
```

A.4.0.2 Discontinuous current conduction mode

```
%initliase local variables
L = (Lsys*2)+ Lfilter; % total inductance before bridge, for dis_con mode
R = R*2;
t_fin = 100e-3; %this value gives a good comprimise between time and accuracy
t = ts;
%initial conditions
col = 2;
v_dc = mag(2,1)*sqrt(3);
i_dc = 0;
%run loop
while t ≤ t_fin %if vdc is greater than system and the input current is zero
```

```
if v_dc(col-1,1) > distorted_sin_three_phase(mag,angle_rad,t,no_of_harms)
    & i_dc(col-1,1) ≤ 0 %discharge
    Req = ((v_dc(col-1,1))^2)/P_rated;
    v_dc(col,1) = v_dc(col-1,1)*exp(-ts/(Req*Cdc));
    i_dc(col,1) = 0;
    t = t + ts;
    col = col + 1;
 else %charge
    t = t + ts;
    Req = ((v_dc(col-1,1))^2)/P_rated;
    E = 325;
    vrect = distorted_sin_three_phase(mag,angle_rad,t,no_of_harms);
    [IV] = solvediff_SMPS_new(v_dc(col-1,1),i_dc(col-1,1),Cdc,L,..
    ..R,ts,vrect,Req);
    i_dc(col,1) = IV(2,1);
    v_dc(col,1) = IV(2,2);
    col = col + 1;
    end
end
%need to get correct pulses
t = 0:ts:10e-3;
t = t';
out(:,1) = t;
out(:,2) = i_dc(round((col-1-(10e-3/ts))):col-1,1);
out(1:round(1.95e-3/ts),2) = 0;
out(length(out)-round(1.66e-3/ts):length(out),2) = 0;
out(1001:2001,2) = out(1:1001,2) *-1;
data_out = out(:,2);
data_out(:,2) = out(:,2);
end
```

A.4.0.3 Continuous current conduction mode

```
%now set current values other than conduction period to zero
iv(1:round(((1/50)/12)/ts),1) = 0;
iv(round(((5/50)/12)/ts):length(iv),1) = 0;
% %now set charge ramp, from previously used code that found t_com duration
iv(round(((1/50)/12)/ts):round(((1/50)/12)/ts)+round(length(I_charge))-1,1)..
..= I_charge(:,1);
vdc_set = vdc_set ;
%now set ramp down
I_dis_start = iv(round((((5/50)/12)-ts)/ts),1);
t_discharge = ts;
 col=1;
 while t_discharge < 1e-3
```

```
   %sysmmetrically same as charging period
mag_new(:,1) = mag(:,1).*0.0186; %adds diode V drop
vin = distorted_sin_asd(mag,angle_rad,t_new(col+round(start_com/ts)),..
..no_of_harms);
vo =   vin - vdc_set ;
I_discharge(col,2) = I_dis_start - ..
..(vo/R*2)*(1 - exp(-t_discharge/((Lsys*2)/R*2)));
I_discharge(col,1) = t_discharge;
 if  I_discharge(col,2) ≥ 0
     Iin_a_last(col,2) = I_discharge(col,2);
     col = col +1;
     t_discharge = t_discharge +ts;
     else
        break
     end
 end
iv(round((((5/50)/12))/ts):round((((5/50)/12))/ts)+..
..length(I_discharge)-1,1) = I_discharge(:,2);
iv_out(:,2) = [iv(:,1); iv(:,1).*-1; iv(:,1); iv(:,1).*-1];
t_out = 4*ts:ts:40e-3-1*ts;
t_out=t_out';
iv_out(:,1) = t_out;
data_out = [iv_out];
```

A.5 Validation of ASD analytical model, for linear torque, quadratic torque and constant mechanical power loading conditions

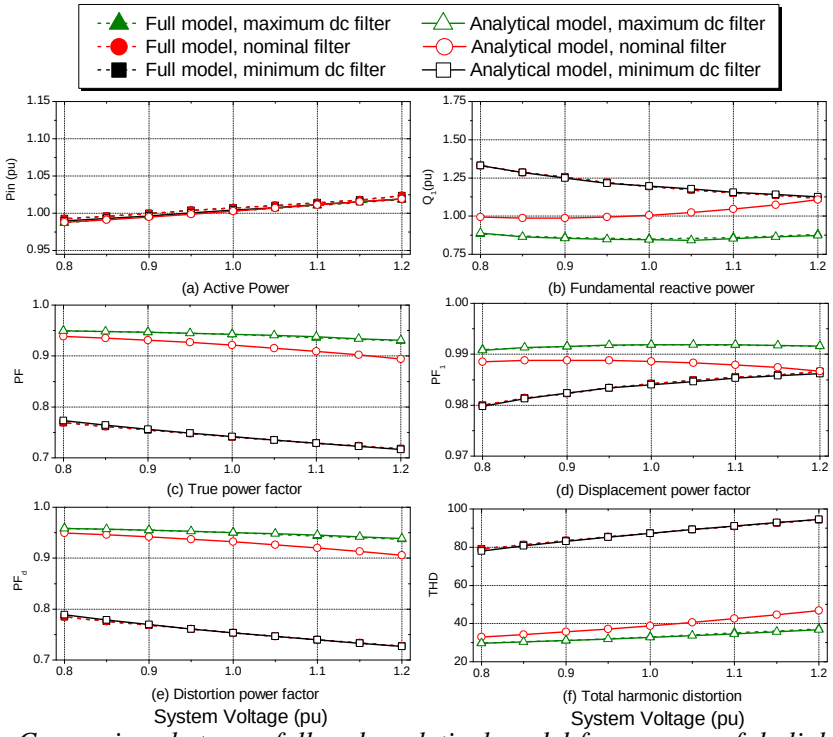


Figure A.8: *Comparison between full and analytical model for a range of dc link component values and motor loaded with linear torque load.*

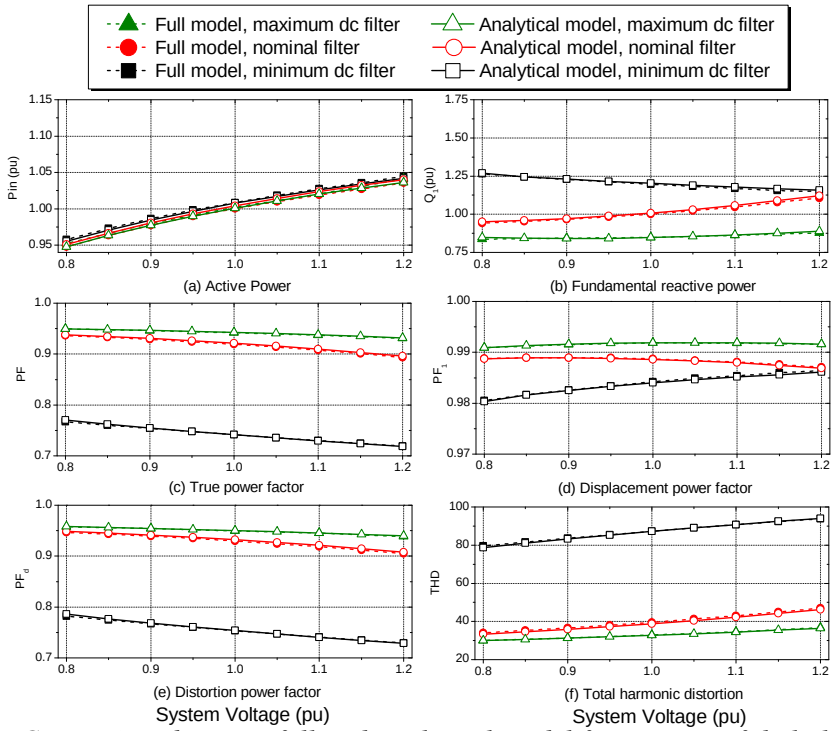


Figure A.9: *Comparison between full and analytical model for a range of dc link component values and motor loaded with quadratic torque load.*

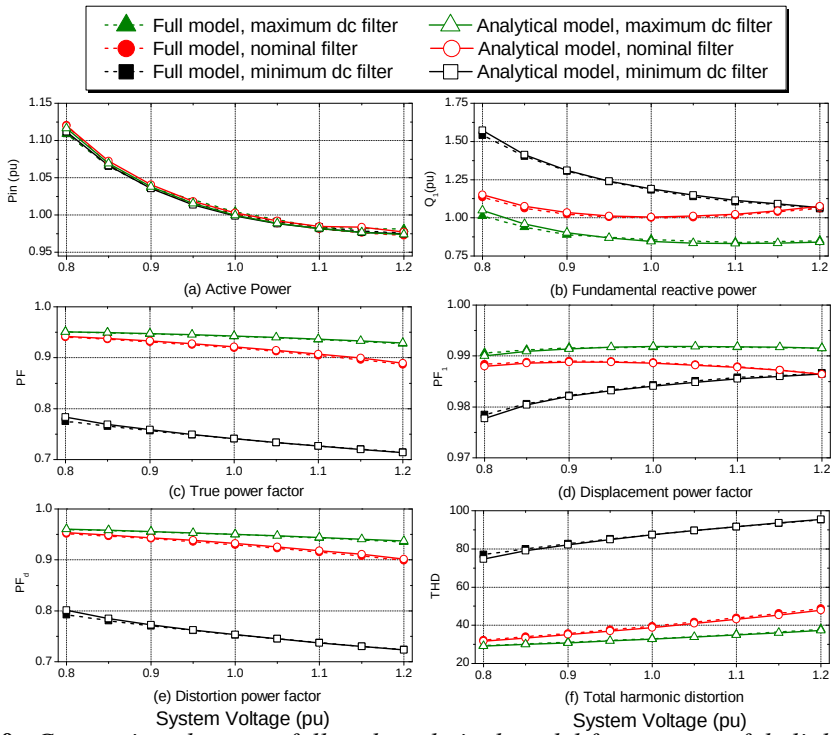


Figure A.10: *Comparison between full and analytical model for a range of dc link component values and motor loaded with constant power mechanical load.*

Appendix B

B.1 PSpice single-phase motor schematic

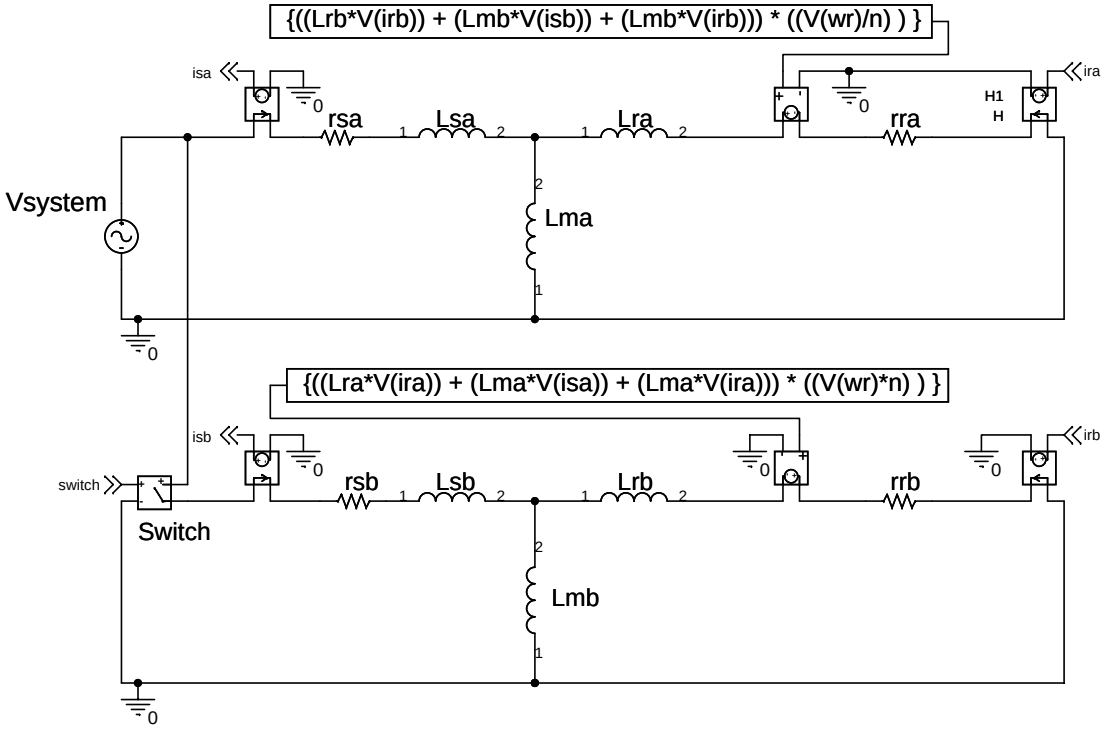


Figure B.1: *PSpice dq model of split-phase single-phase induction motor.*

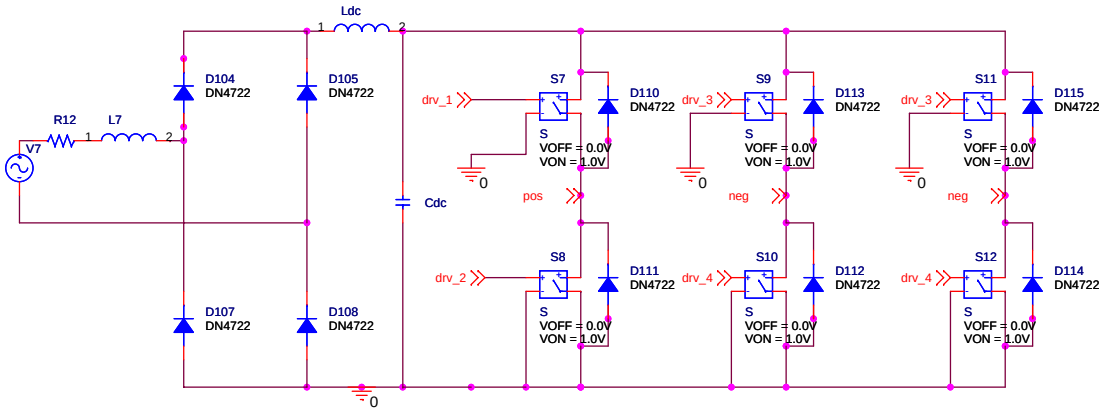


Figure B.2: *PSpice schematic of single-phase drive (connects to three-phase motor).*

B.2 MatLab code implementing equivalent analytical model of SASD

```
col = 2;
%initial conditions
v_dc = 325;
i_dc = 0;
while col ≤ runto

  if v_dc(col-1,1) > abs(distorted_sin(mag,angle_rad,col*ts,no_of_harms))..
       ..& i_dc(col-1,1) ≤ 0
   %discharge
 Req = ((v_dc(col-1,1))^2)/P_SASD;
 v_dc(col,1) = v_dc(col-1,1)*exp(-ts/(Req*Cdc));
 i_dc(col,1) = 0;
 col = col + 1;
 else
    %charge
 Req = ((v_dc(col-1,1))^2)/P_SASD;
 vrect = abs(distorted_sin(mag,angle_rad,col*ts,no_of_harms));

 [IV] = solvediff(v_dc(col-1,1),i_dc(col-1,1),Cdc,L,R,ts,vrect,Req);
 i_dc(col,1) = IV(2,1);
 v_dc(col,1) = IV(2,2);
 col = col + 1;

end
end
t = 0:ts:20e-3;
t = t';
out(:,1) = i_dc(round((col-1-(20e-3/ts))):col-1,1);
out(1:1000,1) = out(1:1000,1) *-1;
out_2(:,1) = i_dc;
out_2(:,2) = v_dc;
```

B.3 Validation of SASD analytical model, for linear torque, quadratic torque and constant mechanical power loading conditions

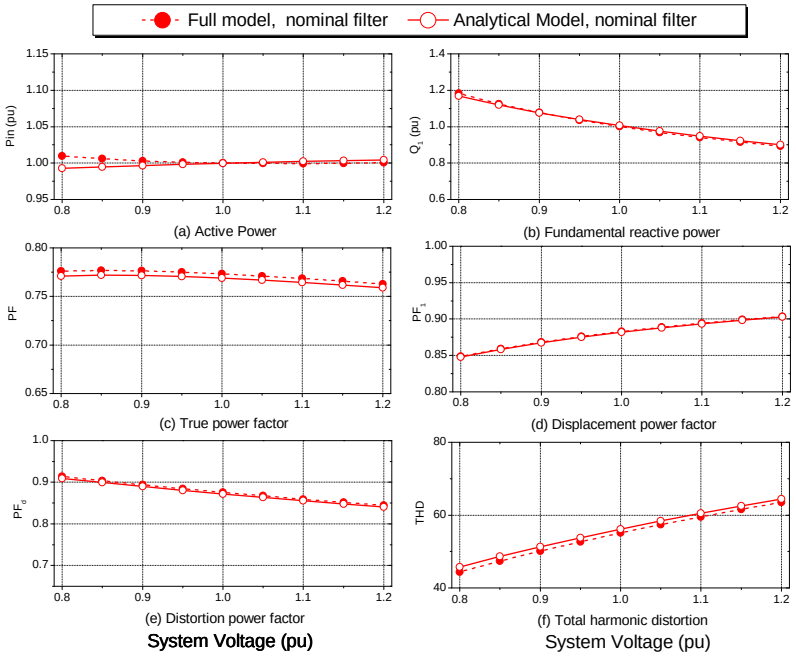


Figure B.3: *Comparison between characteristics of full and analytical models of single-phase open-loop V/HZ ASD mechanically loaded with linear torque for nominal dc link component values.*

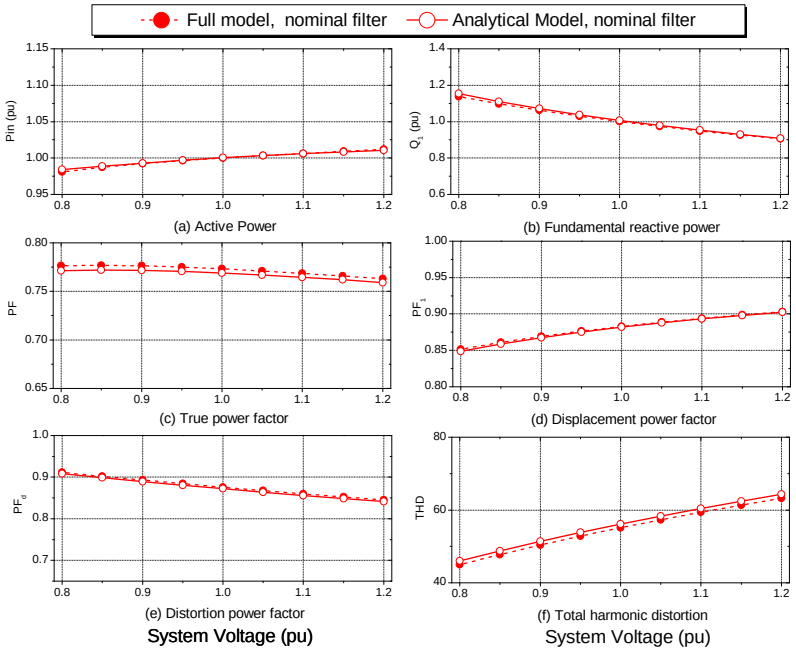


Figure B.4: *Comparison between characteristics of full and analytical models of single-phase open-loop V/HZ ASD mechanically loaded with quadratic torque for nominal dc link component values.*

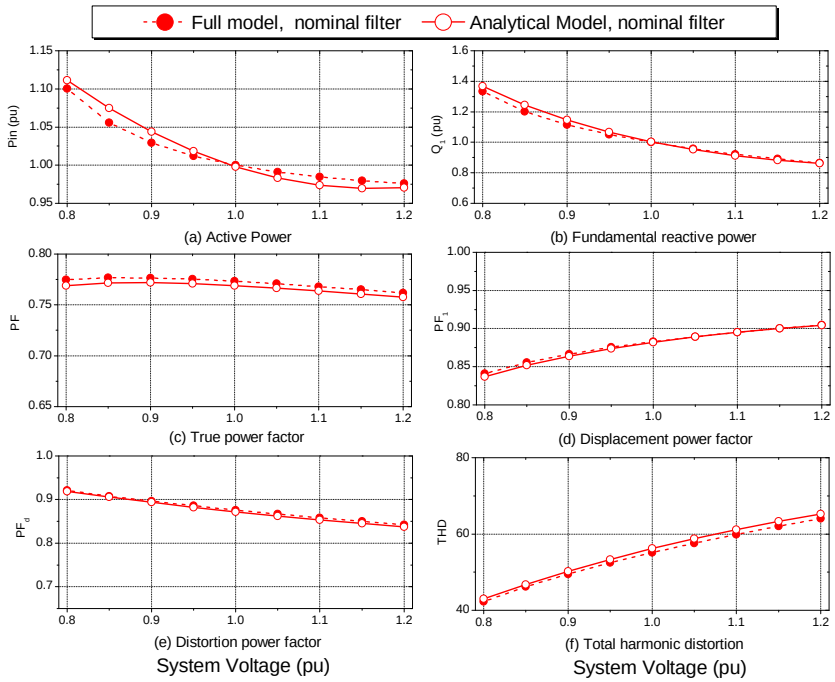


Figure B.5: *Comparison between characteristics of full and analytical models of single-phase open-loop V/HZ ASD mechanically loaded with constant mechanical power load for nominal dc link component values.*

Appendix C

C.1 Lighting chapter MatLab code

C.1.1 MatLab cycle by cycle RMS code

```
%red in data file
data_file = dlmread('v1.2_I_and_Vdc.txt', '', 1,0 );%reads in the data file
%setup data structure
count = 1;
 vdc(:,1) = data_file(:,1);
 vdc(:,2) = data_file(:,2);
 I(:,1) = data_file(:,1);
 I(:,2) = data_file(:,3);

%find gradient
 grad_1 = diff(I);
 % find sign of gradient
 while count ≤ length(grad_1)
 grad_sign(count,1) = find_sign(grad_1(count,2));
 count = count +1;
 end

 %sort start and finish points
 col=1;
 flag = 0;
 count_1 = 1;
 last_reset = 1;

while count_1 < length(grad_sign)
 if grad_sign(count_1,1) == 1 && flag ==0
     start(col,1) = count_1; %start of cycle

     flag = 1;
     col=col+1;
     count_1 = count_1+1;
     last_reset = 1;

 else if grad_sign(count_1,1) == -1 %&& last_reset > 20
         flag =0;
```

```
          count_1 = count_1+1;
          else
           count_1 = count_1+1;
           last_reset = last_reset + 1;
           end
 end
end
%calculate RMS current for each cycle
for start_cycle = 1:1:length(start)-1
end_cycle = start_cycle + 1;

time = I(start((end_cycle),1),1) - I(start((start_cycle),1),1);

data(:,1) = I(start(start_cycle,1):start(end_cycle,1),1);
data(:,2) = I(start(start_cycle,1):start(end_cycle,1),2);
data(:,3) = vdc(start(start_cycle,1):start(end_cycle,1),2);

[I_rms,vdc_rms,P] = P_calc(data,time);
mean_I = mean(data(:,2));

Results(start_cycle,1) = I_rms;
Results(start_cycle,2) = vdc_rms;
Results(start_cycle,3) = P;
Results(start_cycle,4) = mean_I;

data=[];

end
%sort into charging or discharging
count_vrms = 1;
grad_vrms = diff(Results(:,2));

while count_vrms ≤ length(grad_vrms)
 grad_sign_vdc(count_vrms,1) = find_sign(grad_vrms(count_vrms,1));
 count_vrms = count_vrms +1;
end

count_charge_discharge = 1;
discharge_count = 1;
charge_count = 1;
while count_charge_discharge ≤ length(grad_sign_vdc)
    if grad_sign_vdc(count_charge_discharge,1) == -1
        discharge(discharge_count,1:4) = Results(count_charge_discharge,1:4);
        discharge_count = discharge_count + 1;
        count_charge_discharge = count_charge_discharge +1;
    else
        charge(charge_count,1:4) = Results(count_charge_discharge,1:4);
        charge_count = charge_count +1;
```

```
        count_charge_discharge = count_charge_discharge +1;
    end
end
```

C.1.2 MatLab implementation of CFL equivalent analytical model

```
function [out] = lamp_model(Cdc,L,E,R,P_rated)
%outputs, time and Iac
% Initiliasise varaibles
A=-1;
ts = 1e-5;
vint = E;
no_cycles = 8; %enugh for steady state
 time = 0; %time is start point * supply frequency
 voltage = 0;
 current = 0;
flag1 = 0;
no_cycles = no_cycles+1;
t_int = ts;
vend = vint;
V_int = vend;
cycles = 1;
f = 50; %system frequency
w = 2*pi*f;

%equivalent load;
Rbase_old = 6742; %based on(279^2)/11.5449 from generic model
V_DC_base = 279.5; %based on testing a range of CFL
Rbase_new = (V_DC_base^2) / P_rated;

mult_factor = Rbase_new/Rbase_old; %this converts from old base to new base

%discharging
c_A = -511.66*mult_factor;
c_B = 27.88*mult_factor;
c_C = -0.0033*mult_factor;

%charging
c_D = 500*mult_factor;
c_E = 10.9*mult_factor;
c_F = 0.03237*mult_factor;
```

```
while cycles < no_cycles
t_fin = ((0.5/f)*(cycles+1));
col = 1;
t(col,1) = (ts)+ ((cycles)*(0.5/f));
V2_1(col,1) = vend;
flag = 0;

while V2_1(col,1) ≥ abs(E*sin(w*t(col,1))) && flag1 == 0 %discharge stage

    col=col+1;
    t(col,1) = t(col-1,1) + ts;
    %calcuates Req1 frm previous value of cdc
    Req_1 = c_A + c_B*V2_1(col-1,1) + c_C*V2_1(col-1,1)*V2_1(col-1,1);
    ;%calulates new dc link voltage
    V2_1(col,1) = V2_1(col-1,1)*exp(-ts/(Req_1*Cdc))
    I2_1(col,1) = 0;
    V_int = V2_1(col,1);
    t_int = t(col,1);

%need to jump out of loop if no conduction period in loop
if t(col,1) ≥ t_fin; %
    vend  = V2_1(col,1);
    break
    end

end
  flag1 = 1;
flag=1;
col = 1;
%charge period
[T2, IV2] = solvediff_lamp(t_int,t_fin,V_int,Cdc,L,R,c_D,c_E,c_F,w,E,ts);

while col ≤ length (IV2)

    if IV2(col,1) ≥ 0 && flag == 1
        I2_2(col,1) = IV2(col,1);
        V2_2(col,1) = IV2(col,2);
        V_dis_start2 = IV2(col,2);
        t_dis_start2 = T2(col,1);
        col  = col + 1;
    else
        flag = 0;
        I2_2(col,1) = 0;
        %calcuates Req1 frm previous value of cdc
       Req_1 = c_A + c_B*V2_2(col-1,1) + c_C*V2_2(col-1,1)*V2_2(col-1,1);
       %calulates new dc link voltage
        V2_2(col,1) = V2_2(col-1,1)*exp(-ts/(Req_1*Cdc)) ;
        vend = V2_2(col,1);
```

```
        col = col + 1;
        end

end
T2 = [t;T2];
I2 = [I2_1 ; I2_2];
V2 = [V2_1 ; V2_2];

%save cycles
cycles = cycles + 1;
flag1 = 0;
time =    [time ; T2];
current = [current ; (I2*A)];
voltage = [voltage ; V2];
A = A*-1;

t = [];
T2 = [];
I2_1 = [];
I2_2 = [];
V2_1 = [];
V2_2 = [];
V2 = [];
I2 = [];
end
out = 0:ts:20e-3;
out = out';
out(:,2) = current(length(current)-(20e-3/ts):length(current),1);
```

Appendix D

D.1 MatLab code implementing aggregation of generic analytical models

```
vs_count = 1;
for Vsys = [0.8:0.1:1.2]

%system impedance
Rsys=0.25*0.6;
j=0.23*0.6;
Lsys = j/(2*pi*50);
THD_last = -5;
%%%%%%%%%%READ IN VOLTAGE

%sinusodial voltage and current, can also make non-sinu of required
mag_voltage = zeros(50,1);
angle_voltage = zeros(50,1);
% % % % %This one is a sinusiod
mag_voltage(:,1) = 0;
mag_voltage(2,1) = Vsys*325;
angle_voltage(:,1) = 0;
mag = mag_voltage;
angle_rad =angle_voltage;

%%%%%%%%
no_of_harms = 50; %
colres=1;
ts = 1e-5;
scaling_factor = 50;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

Percentage_SMPS = 25.*scaling_factor; %actual percentage power drawn by SMPS
SMPS_loading = 0.4; %the loading of rated power on the SMPS
percent_SMPS_LP = 0.4068*Percentage_SMPS; %how many are LP
percent_SMPS_HP = 0.4929.*Percentage_SMPS; %how many are HP
percent_SMPS_active = 0.10.*Percentage_SMPS;
        P_SMPS_in_mix = 250; %the typical rated power of the SMPS in the load mix.
```

```
%ASD
Percentage_ASD = 20*0.2*3.*scaling_factor; %nb increase ASD by three times to give correct
%Percentage_ASD = 0;
    percent_CT = 0.0.*Percentage_ASD;
    percent_LT = 0.0.*Percentage_ASD;
    percent_QT = 0.0.*Percentage_ASD;
    percent_CP = 0.5.*Percentage_ASD;
    percent_CP_NF = 0.5.*Percentage_ASD;

%Directly connected three-phase motors
Percentage_DC3 = 20*0.8.*scaling_factor;
    percent_DC3_CT = 0.5.*Percentage_DC3; %percentage cosntant torque
    percent_DC3_LT = 0.0.*Percentage_DC3;
    percent_DC3_QT = 0.5.*Percentage_DC3;
    percent_DC3_CP = 0.0.*Percentage_DC3;
    percent_DC3_HP = 0.0.*Percentage_DC3; %percentage higher power

%SASD
Percentage_SASD = 26*0.20.*scaling_factor;
P_SASD_in_mix = 961; %this is based on 1hp SASDs
    percent_CT_SASD = 0.0.*Percentage_SASD;
    percent_LT_SASD = 0.0.*Percentage_SASD;
    percent_QT_SASD = 0.0.*Percentage_SASD;
    percent_CP_SASD = 1.0.*Percentage_SASD;
    percent_advanced_SASD = 0.0.*Percentage_SASD;
percent_LP_SASD = 0.0.*Percentage_SASD;


   %SPIM
Percentage_SPIM = 26*0.8.*scaling_factor;
    percent_RSIR_CT = 0.75*Percentage_SPIM;
    percent_RSIR_LT = 0.0.*Percentage_SPIM;
    percent_RSIR_QT = 0.0*Percentage_SPIM;
    percent_RSIR_CP = 0.0.*Percentage_SPIM;
    percent_RSCR_CT = 0.25.*Percentage_SPIM;
    percent_RSCR_LT = 0.0.*Percentage_SPIM;
    percent_RSCR_QT = 0.0.*Percentage_SPIM;
    percent_RSCR_CP = 0.0.*Percentage_SPIM;


%CFL lighting
Percentage_CFL = 1.*scaling_factor;

% Resisitive load:
%made up of 12.92% lighting,
Percentage_resisitive = 28.*scaling_factor;
```

```
%%%%%%%%%%CALL MODELS %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%call CFL load
agg_CFL = CFL_load(Lsys,Percentage_CFL,Vsys,mag,angle_rad,no_of_harms);

%call ASD load
[agg_ASD ,agg_ASD_con,agg_ASD_discon]= call_ASD_model(ts,Vsys,Lsys,Rsys,..
..percent_CT,percent_LT,percent_QT,percent_CP,percent_CP_NF,mag,..
..angle_rad,no_of_harms);

%call SASD load
[agg_SASD, agg_SASD_LP] = call_SASD(Vsys,Lsys,Rsys,percent_CT_SASD,..
percent_LT_SASD,percent_QT_SASD,percent_CP_SASD, percent_advanced_SASD,..
..percent_LP_SASD,P_SASD_in_mix,mag,angle_rad,no_of_harms);

%Call SMPS model
[agg_SMPS,agg_SMPS_LP,agg_SMPS_HP,agg_SMPS_APFC] = call_SMPS(Vsys,Lsys,..
..Rsys, percent_SMPS_LP, percent_SMPS_HP,percent_SMPS_active,..
..P_SMPS_in_mix,SMPS_loading,mag,angle_rad,no_of_harms);


%Call directly connected three-phase
agg_DC3 = three_DC(Vsys,percent_DC3_CT,percent_DC3_LT,percent_DC3_QT,..
..percent_DC3_CP,percent_DC3_HP,mag,angle_rad);

%call directly connected single-phase
agg_SPIM = SPIM(Vsys,percent_RSIR_CT,percent_RSIR_LT,percent_RSIR_QT,..
..percent_RSIR_CP,percent_RSCR_CT,percent_RSCR_LT,percent_RSCR_QT,..
..percent_RSCR_CP,mag,angle_rad);

%call resisitive load
agg_resist = resisitive(Vsys,Percentage_resisitive,mag,angle_rad,no_of_harms);

%Add the invidual load currents together
aggregate_current(:,1) = agg_CFL + agg_ASD(:,1) + agg_SASD(:,1) + ..
..agg_DC3(:,1) + agg_SPIM(:,1) + agg_resist(:,1) + agg_SMPS(:,1);
end
```

Appendix E

E.1 List of publications from research presented in thesis

- C. Cresswell, S. Djokic, and S. Munshi, Analytical modelling of adjustable speed drive load for power system studies, in Proc. of Power Tech, Lausanne, 2007, pp. 18991904.
- C. Cresswell and S. Djokic, Representation of directly connected and drive-controlled induction motors. part 2: Three-phase load models, in Proc. of the 2008 International Conference on Electrical Machines, Vilamoura, Portugal, paper 1203.
- S. Djokic, S. Munshi, and C. Cresswell, The influence of overcurrent and undervoltage protection settings on asd sensitivity to voltage sags and short interruptions, in Proc. of 4th IET Conference on Power Electronics, Machines and Drives, PEMD, 2008, pp.130134.
- C. Cresswell and S. Djokic, Representation of directly connected and drive-controlled induction motors. part 1: Single-phase load models, in Proc. of the 2008 International Conference on Electrical Machines, Vilamoura, Portugal, paper 1202.
- C. Cresswell and S. Djokic, The analysis of the occurrence of high in-rush currents in dc power supplies, in Proc. of 4th IET Conference on Power Electronics, Machines and Drives, PEMD, 2008, pp. 441445.
- C. Cresswell, S. Djokic, K. Ochije, and D. Macpherson, Modelling of non-linear electronic loads for power system studies: A qualitative approach, in Proc. of International Conference on Electricity Distribution, CIRED, Vienna,, 2007, Paper 458.
- C. Cresswell and S. Djokic, Steady state models of low-energy consumption light sources, in Proc. of 16th Power Systems Computation Conference, PSCC 2008, Glasgow, Paper 84.

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